ANALOG TO DIGITAL CONVERTER

A thesis submitted
In partial fulfilment of the requirements
for the Degree of
MASTER OF TECHNOLOGY

by

VISHNU PRASAD NAMDEO
to the
Department of Electrical Engineering
Indian Institute of Technology, Kanpur

December 1967

CERTIFICATE

Certified that the present work has been carried out under my supervision and that this work has not been submitted elsewhere for a degree.

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ACKNOWLEDGMENTS

The author is very much indebted to Dr. T.R. Viswanathan for his enthusiasm, advice, suggestions and critical appraisal while guiding this problem.

The author is grateful to the department of Electrical Engineering, Indian Institute of Technology, Kanpur for the facilities provided.

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Various methods of Analog to Digital Conversion are discussed. An A/D converter circuit based on a scheme suggested by D. Savitt is discussed in detail. Some modifications to Savitt's scheme are suggested. The circuit is designed using transistors.

CHAPTER - I

INTRODUCTION

1.1. GENERAL

A tremendous amount of progress has been made in the technology of information processing machines during the last decade. These are broadly classified as analog and digital techniques depending upon the manner in which they handle the data to be processed. The digital computers deal with discrete quantities whereas analog computers deal with continuous physical variables. The digital machines can do a wider variety of jobs than can the analog ones. From the point of view of cost, digital machines are preferred, for, the cost of attaining greater precision in a digital machine increases linearly whereas in the case of analog computation the cost increases exponentially with the precision. With the advent of semiconductor devices, effective steps have been taken in the miniaturisation of the system thus providing a facility of accommodation of larger number of units in the same available space. When the accuracy requirement is stringent (less than 1%) it is advantageous to use digital information processing techniques.

The information from a physical system, which is an analog signal, may be mechanical, photometeric, hydraulic, etc. If it is not electrical then a suitable transducer is used to get the analogous electrical form which can be handled much more easily. Since the digital information processing equipment deals with numbers, a device is needed which links the analog signal to the digital information processor. This is termed Analog to

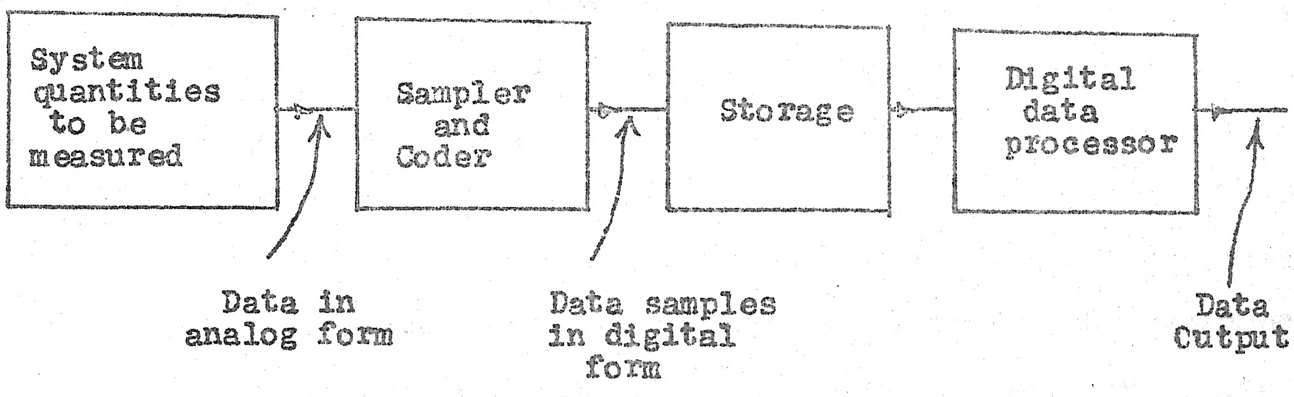


FIG. 1. ANALOG TO DIGITAL CONVERSION

Digital Converter (A/D) or Encoder. The device which performs the inverse operation is termed as Decoder or Digital to Analog Converter (D/A).

1.2. ANALOG SIGNALS AND QUANTIZATION

Analog representation is a continuous one. It can take an infinite number of values. Because of the very nature of digital representation the conversion of an analog signal to a corresponding number can only be an approximation. The degree of approximation depends on the number of digits used. This process of approximation is called quantization.

Digital equipments need a definite amount of time to process the information. Since the inputs change continuously, the equipment must ignore variations in input till the present computation is over. So the reference to the input is intermittent. This process is termed sampling or quantization in time. The block diagram in Fig. 1 gives the steps needed to achieve this. The process of obtaining samples from a continuous signal at discrete time intervals results in the loss of information unless it is done in accordance with the Sampling Theorem[1]. It is necessary to take samples at more than two points per cycle of the highest significant frequency component in a signal in order to recover that signal. Hence the sampling frequency should be at least two times of the highest frequency component contained in the original signal.

1.3. DIGITAL REPRESENTATIONS

1.3.1. General:

The most widely used number systems are positional systems. In these, according to some general agreement, the position of the

various digits marks the significance to be attached to each digit. In the case of familiar decimal system, a sequence

$$a_n \; a_{n-1} \; a_{n-2} \; \ldots\ldots \; a_2 \; a_1 \; a_0 \; . \; a_{-1} \; a_{-2} \qquad \text{---} \qquad (a)$$

is always understood to mean

$$a_n \times 10^n + a_{n-1} \times 10^{n-1} + \ldots\ldots + a_2 \times 10^2 + a_1 \times 10^1$$
$$+ a_0 \times 10^0 + a_{-1} \times 10^{-1} + a_{-2} \times 10^{n-2} + \qquad \text{---} \qquad (b)$$

If the weights attached to each a_k are clearly stated then there is no necessity to write the number sequence in any particular order. A sequence $a_1 \times 10^1 + a_{n-1} \times 10^{n-1} + a_2 \times 10^2$ etc. will mean the same as the order sequence (b) if all the terms are included. If, however, the sequence is always placed in the same order then the weighting factors associated with each digit need not be explicitly stated. But then a digit must be included for each position whether units of that weight are present in the number or not. Thus $5 \times 10^4 + 3 \times 10^3 + 4 \times 10^0$ is written in positional notation as 53004 instead of 534. This is necessary to preserve the positional significance of the digit. The decimal system is useful in computer applications mainly because it is generally well understood. The number 10 is called the radix or base of the decimal system. The radix of any system is always equal to the number of characters used in that system.

1.3.2. Binary System:

The system using radix 2 is called a binary system. Only two digits 0 and 1 are used. They are called bits. The digit position determines the power of 2 by which it should be multiplied. For example, the number 1001.1 actually corresponds to $1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1}$ and its decimal

equivalent number is 9.5. This system is economical than the decimal system as far as the total number of digits per position is concerned (2 for binary, 10 for decimal); however, the binary system requires more bits than the digits required by decimal to represent the same number. A computer may do as many as 10^5 arithmetic operations per second, and a problem that may run for a week is not unusual. This will amount to approximately 15×10^{19} arithmetic operations which must be performed without errors in order to obtain reliable and correct answers. This necessitates very careful design of the individual circuits which perform these operations. The general result of such stringent requirement is that in the present state of computer technology, most of the machines, whatever radix they employ, make use of a number representation based upon the binary symbols. That is, each individual circuit is either 'ON' or 'OFF', except during a transition period. In other words, the machine has to distinguish as well as to deal with only two symbols. Furthermore with reference to the binary addition table given in Table 1.1 and multiplication table shown in Table 1.2, it is evident that additive and multiplicative operations involve only simple logical decisions which are performed with logical gating circuits.

	0	1
0	0	1
1	1	10

Table 1.1
Binary Addition of Digits

	0	1
0	0	0
1	0	1

Table 1.2
Binary Multiplication of Digits

Similar operations in the decimal system will be lot more complex and will require complex hardware.

1.3.3. Other Widely Used Systems:

The large number of characters needed to represent numbers of reasonable size makes it difficult for individuals to write and understand binary numbers. For this reason radices related to the binary system have been used. Most binary computers have a mode of input and output which uses the octal (radix 8) number system. The octal system uses the digits from 0 through 7 and the radix 8. Large numbers can be more effectively read and handled when they are first converted into octal. Also it is generally easier to convert a decimal number into octal rather than binary; the conversion from octal to binary can then be accomplished very easily.

When in decimal system binary bits equivalent to each digit are placed in place of the digit itself, the resulting system is termed as Binary Coded Decimal System (BCD). $1074_{(10)}$ is written in BCD as $0001 \quad 0000 \quad 0111 \quad 0100_{(BCD)}$.

It may be mentioned that conversion between Decimal, Binary, Octal and BCD are often needed and can be performed with the use of diode matrix type of gates.

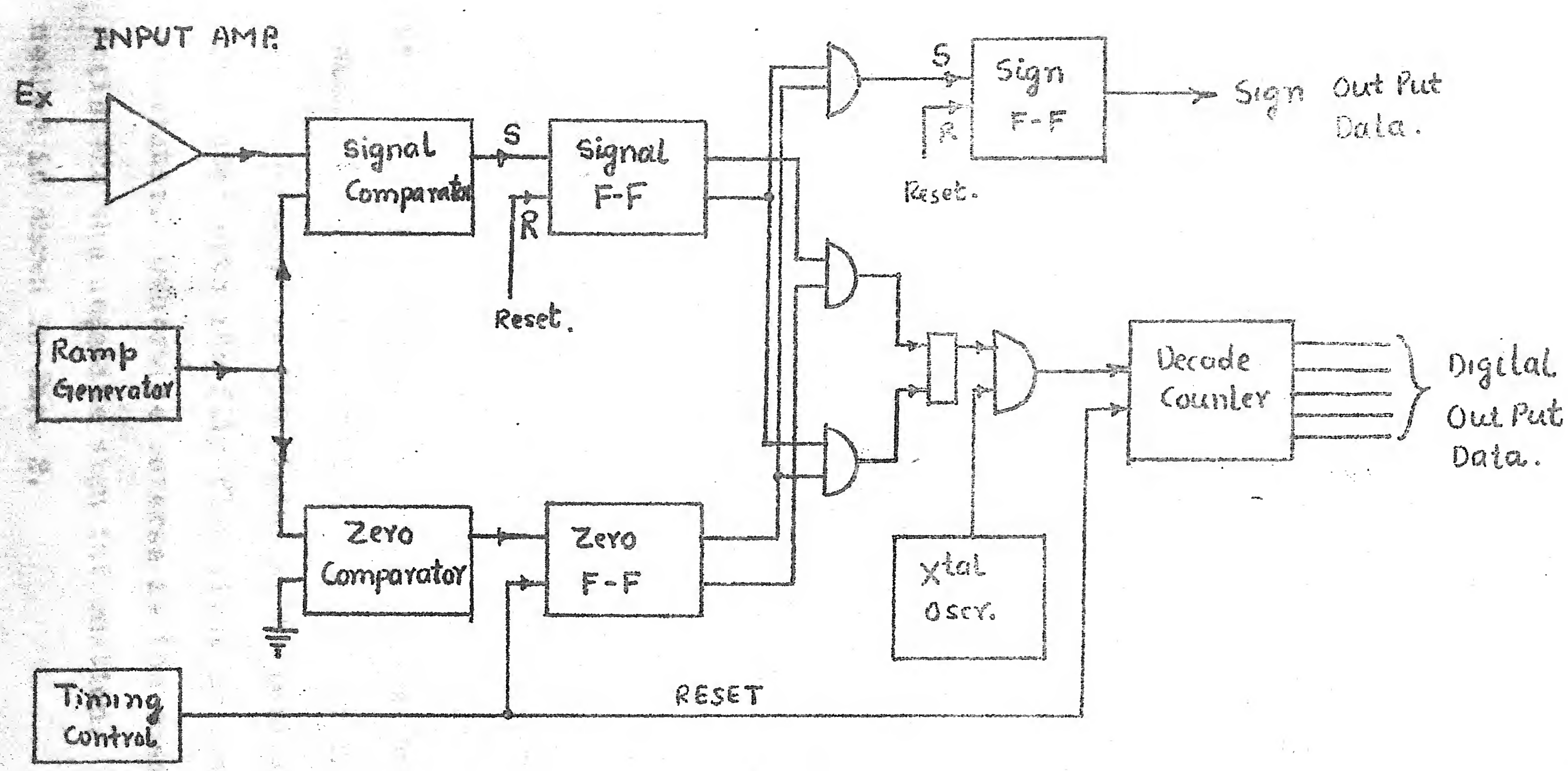


FIG. 2.   TIME BASE RAMP CONVERTER

CHAPTER - II

METHODS OF ANALOG TO DIGITAL CONVERSION

2.1. TIME BASE RAMP CONVERTER

In a ramp function the amplitude of the function at any instant is proportional to the time lapsed from the instant of beginning of the ramp to that particular instant. The unknown analog sample is compared with a locally generated ramp voltage (Fig.2). The time period since the commencement of the ramp to the instant of zero output from comparator is utilised to control the gate between crystal oscillator and the counter. Thus the count registered in the counter is the digital representation of the analog input. The time control unit provides the start pulse for ramp and the reset pulses to the count register before starting a new comparison afresh. Sensing of the sign of the input voltage can be done by comparing the ramp voltage to a zero reference voltage. The signal comparator produces a signal to set the signal flip-flop whenever the ramp is more negative than the incoming unknown voltage. Similarly the zero comparator produces a signal to set the zero flip-flop when the ramp voltage is less than the zero volts. The logic circuitry connecting the F-F to the counter is such that the high frequency pulses from the crystal oscillator reach the counter only when only one of the comparators has set its flip-flop. If the signal is of positive polarity, the signal comparator sets its flip-flop first as compared to the zero comparator. Otherwise reverse is the case and the sign flip-flop registers the negative sign information. The principle of this method in shown in Fig. 2.

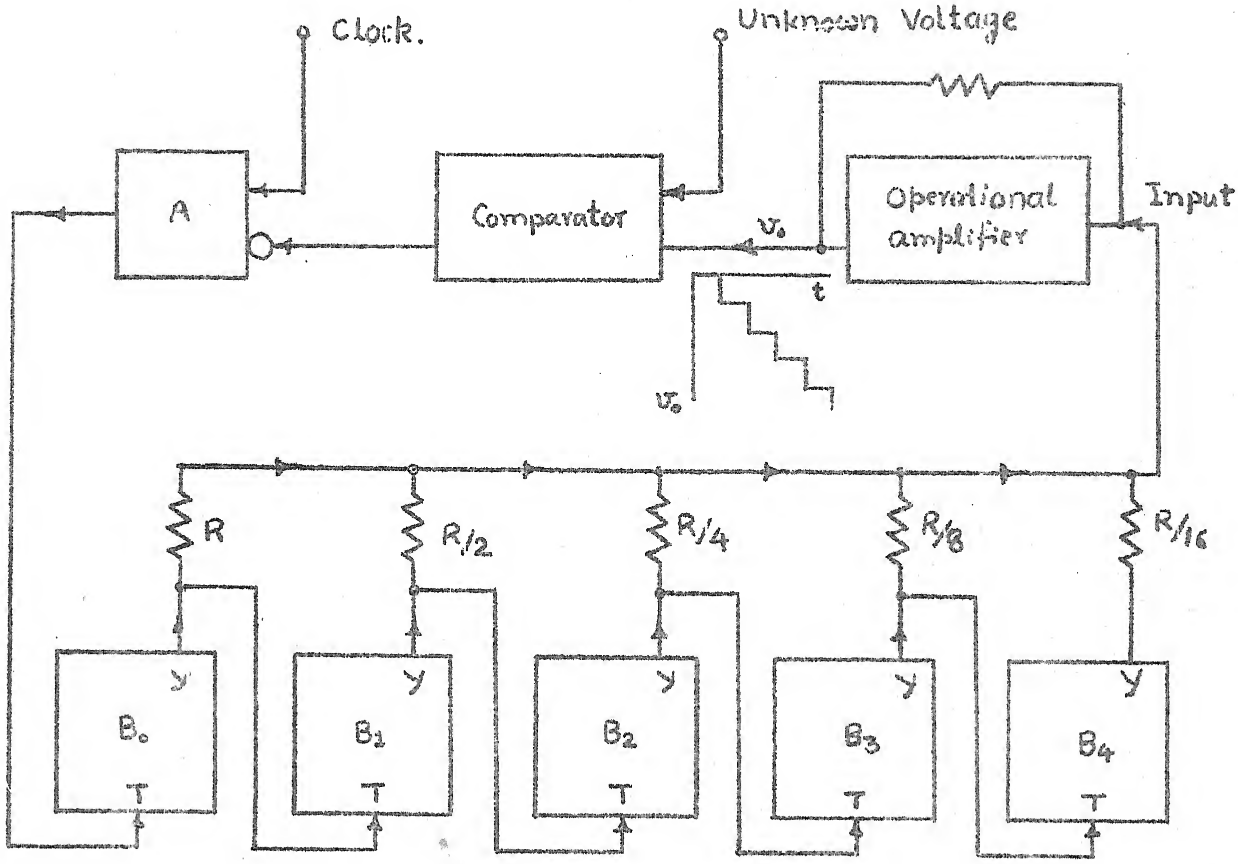


FIG. 3. ANALOG TO DIGITAL CONVERTER USING STAIRCASE VOLTAGE FOR COMPARISON.

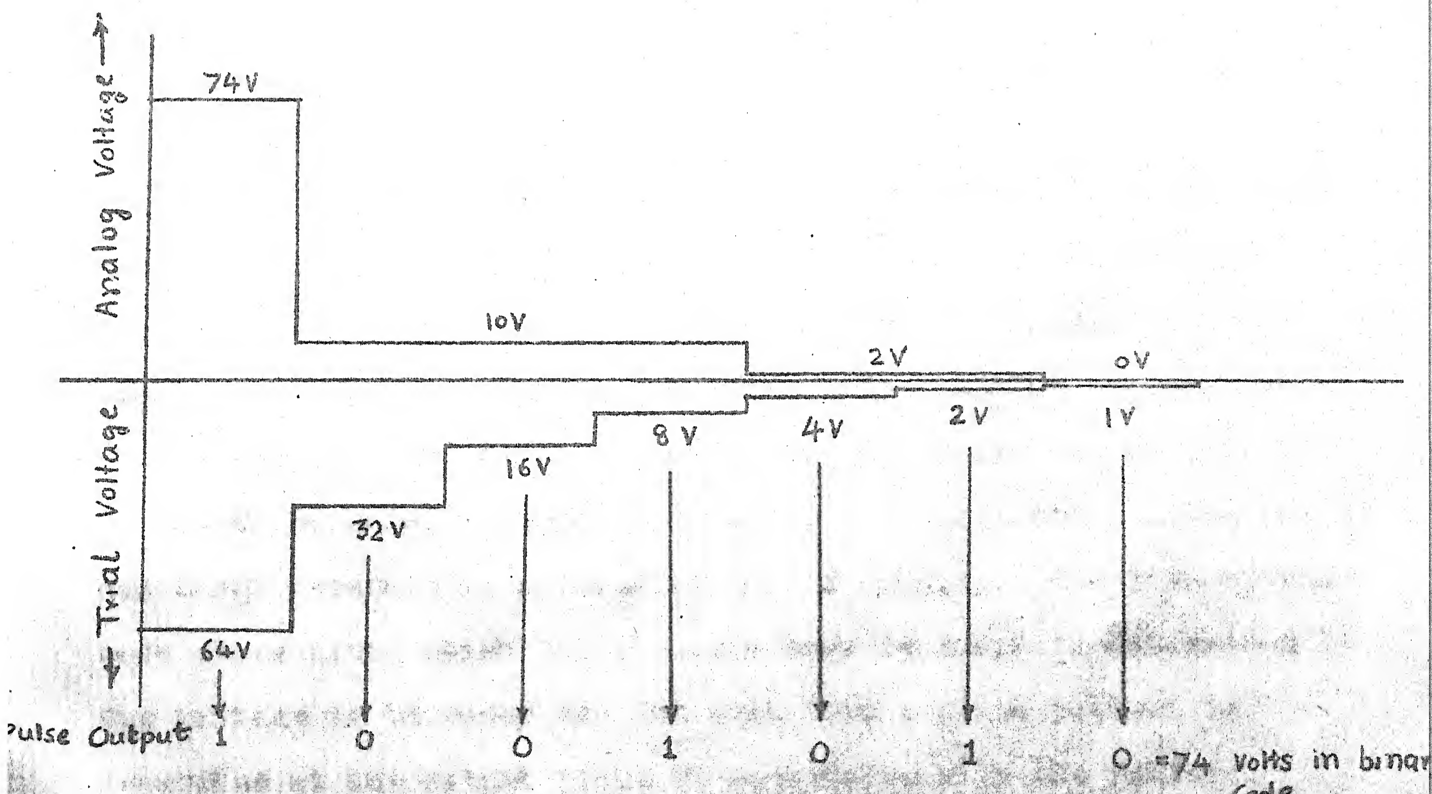


FIG. 4. PRINCIPLE OF A/D CONVERTER USING TRIAL

Instead of using a ramp function a stair case type voltage can be used for comparison with the unknown analog voltage. This stair case voltage is obtained from D/A conversion of the digital output of a counter into which pulses of a constant frequency are fed. The circuit diagram of such an A/D converter is shown in Fig. 3.

2.2. CONVERSION BY TRIAL VOLTAGES

Successive trial voltages, which are weighted or compared against the unknown analog voltage, are chosen to be powers of 2. If the unknown voltage is greater than the trial voltage, the trial voltage is retained and is subtracted from it and a pulse is emitted signifying '1'. If reverse is the case then the trial voltage is thrown away and no pulse is emitted, signifying '0'. Thus if the unknown d.c. voltage is 74 volts, it is successively weighted against 64, 32, 16, 8, 4, 2, 1 volts and the binary output, according to the above rules is 1001010 which is the binary code for 74. The principle of the method is shown in Fig. 4.

2.3. SPATIAL CODING

The coding tube consists of an electron gun and deflection plates similar to the ones in a CR tube. The opening in the aperture plate is in the form of a pattern according to the conventional binary code, as shown in Fig. 5. The column one of the pattern corresponds to 2^0 digit, column 2 to 2^1 digit and so on. The sample to be coded is connected to the Y deflection plates and a saw tooth waveform is applied to the X plates. The line of the code plate along which the electron beam is swept is determined by the voltage to be coded and for each line a pulse pattern is generated at the output plate in accordance with the pattern. The principle of the method is shown in Fig. 6.

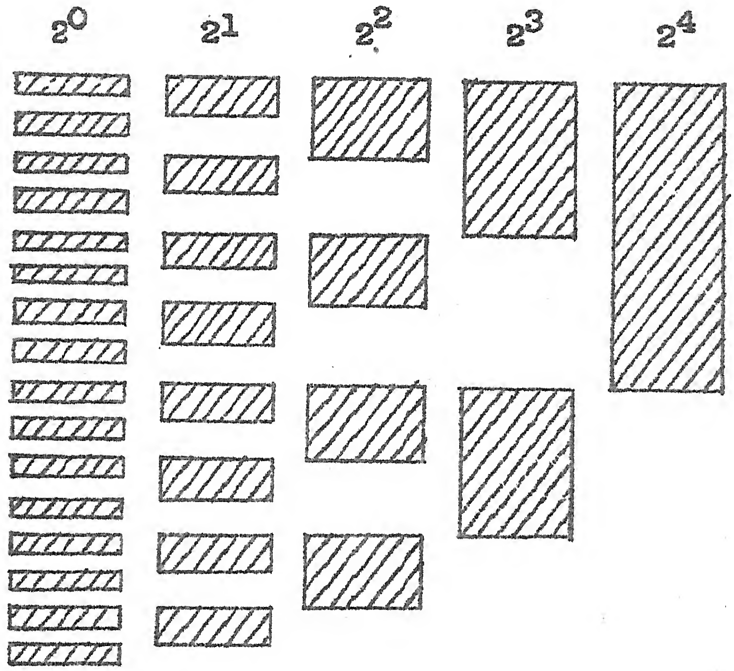


FIG. 5. BINARY PATTERN USED IN SPATIAL CODING.

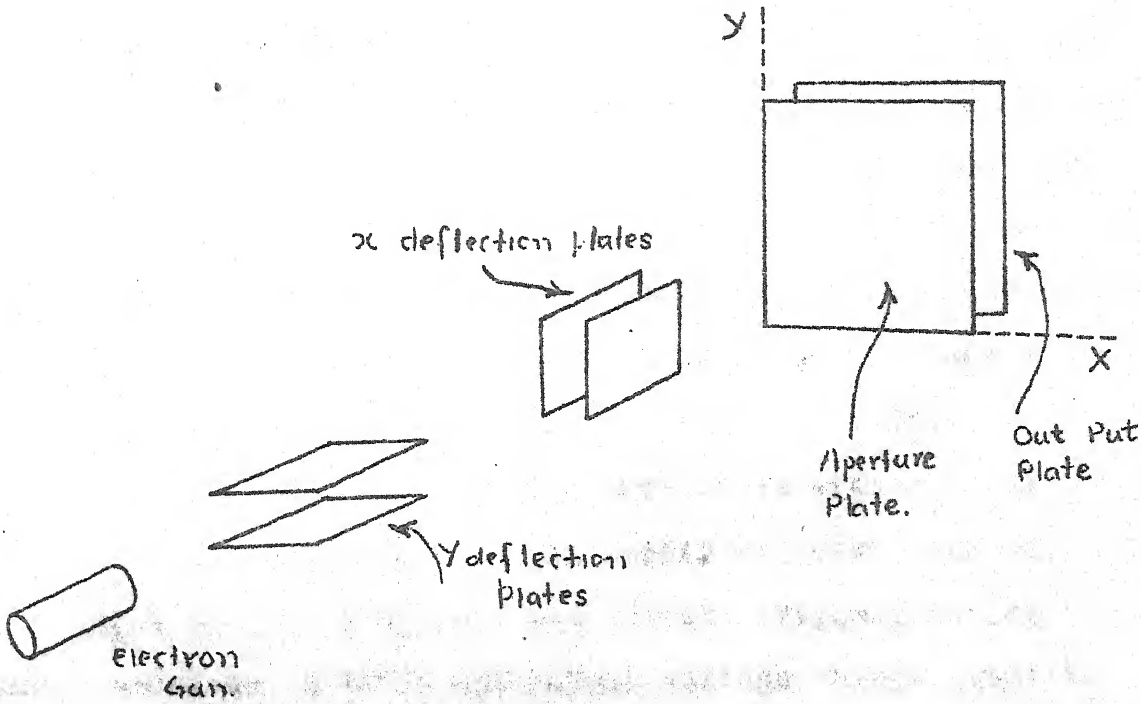


FIG. 6. SPATIAL CODING.

CHAPTER - III

THE DESIGN OF THE ANALOG TO DIGITAL CONVERTER

3.1. BLOCK DIAGRAM OF THE EQUIPMENT AND GENERAL SCHEME OF APPROACH

The block diagram of the instrument is given in Fig. 7. The basic principle of the method adopted here is described by R.P. Sullen[2] as well as by B.D. Smith[3]. An A/D converter based on this principle has also been designed by Donald Savitt[4] using vacuum tube Schmitt triggers as threshold devices.

A block diagram outlining the principle is shown in Fig. 8. Assuming that one has a coding system which quantises the continuous signal into certain number of levels and a decoding system, one can produce, in addition to the digital outputs, a decoded voltage V_1'. This decoded output V_1' differs from the input V, by an amount equal to the quantization error. If the difference of V_1 and V_1' is obtained and amplified, this difference signal can be made to be the input to a similar coding stage, and additional digits can be obtained. The above principle when applied to binary code system, the threshold device used being a Schmitt trigger, results in the basic block diagram as shown in Fig. 9. A binary storage unit to store and display the digital outputs is also included.

A_1 , A_2 , ..., A_n are the amplifiers with gain -1.

A_1' , A_2' , ..., A_n' are the amplifiers with gain -2.

S_1 , S_2 , ..., S_n are the Schmitt triggers having threshold equal to x volts and output voltage change equal to x volts where the maximum input to be handled by the system is slightly less than $2x$ volts.

B_1 , B_2 , ..., B_n are the binaries which store the

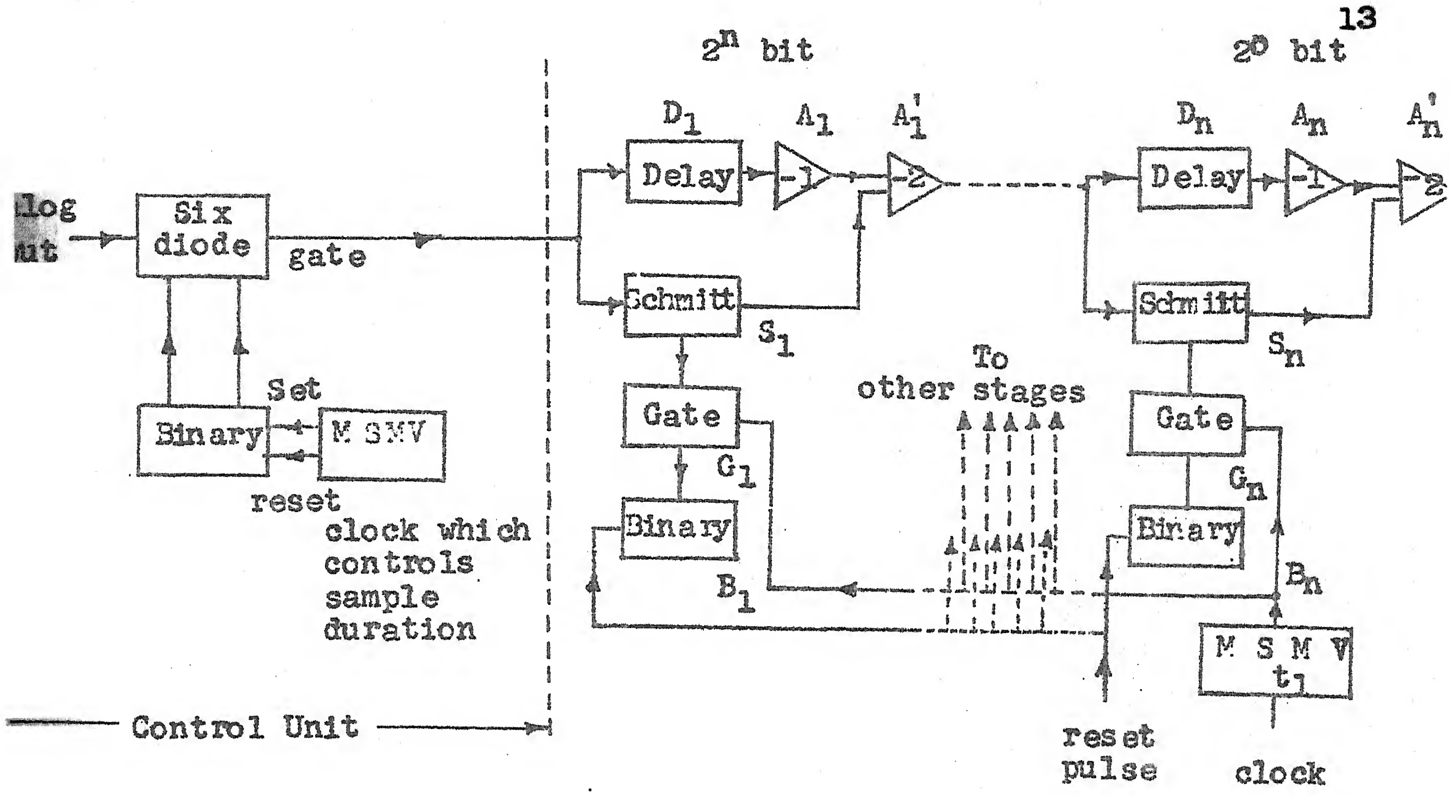


FIG. 7(a). MODIFIED BLOCK DIAGRAM (METHOD II).

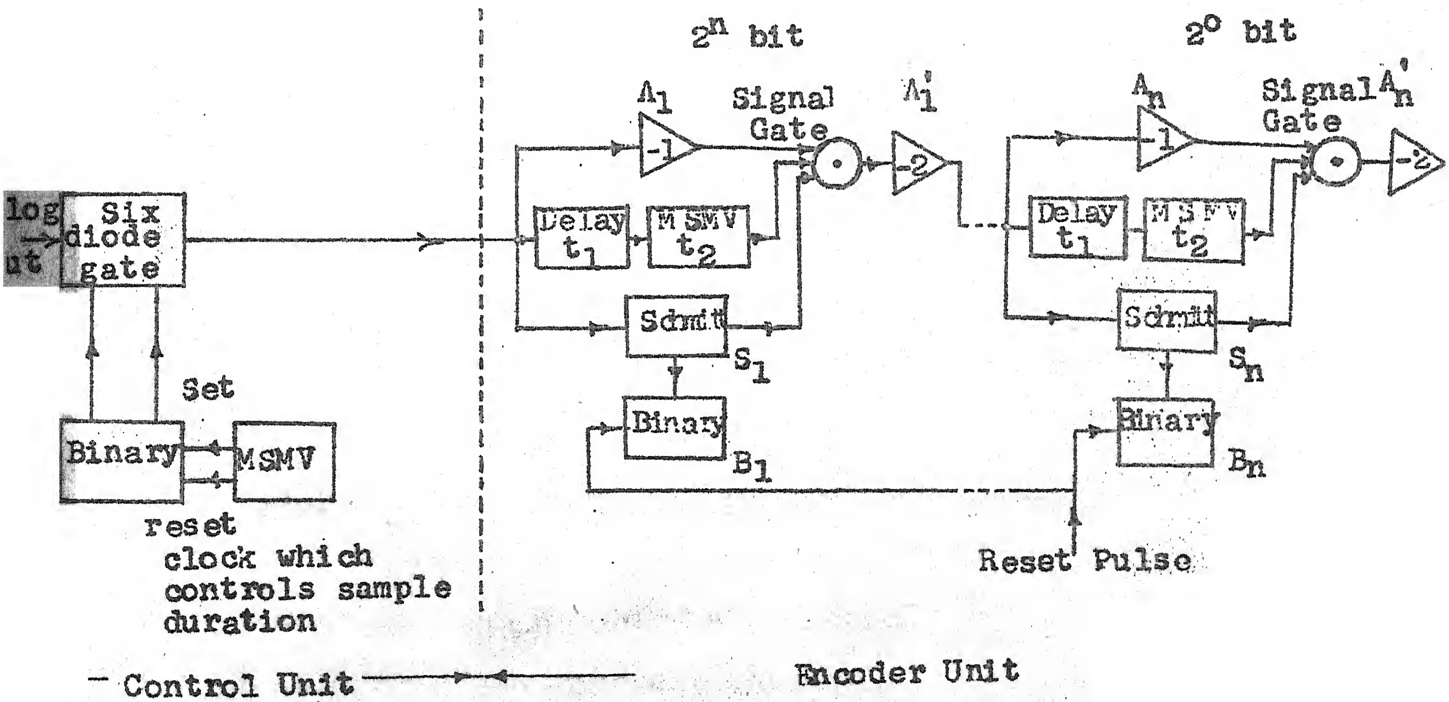


FIG. 7(b). MODIFIED BLOCK DIAGRAM (METHOD I).

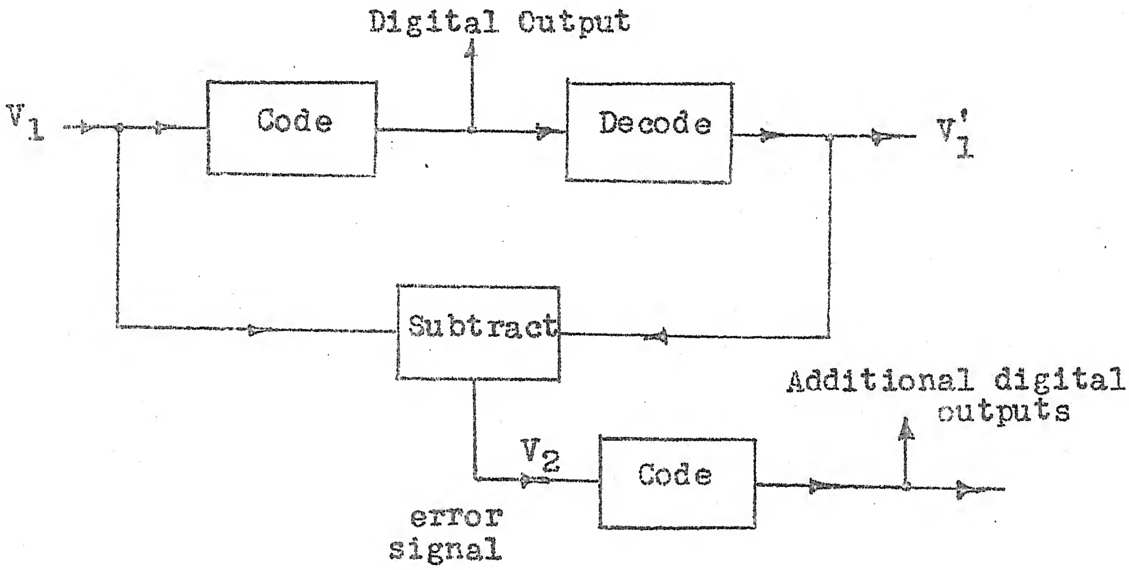


FIG. 8. METHOD OF CASCADING CODERS.

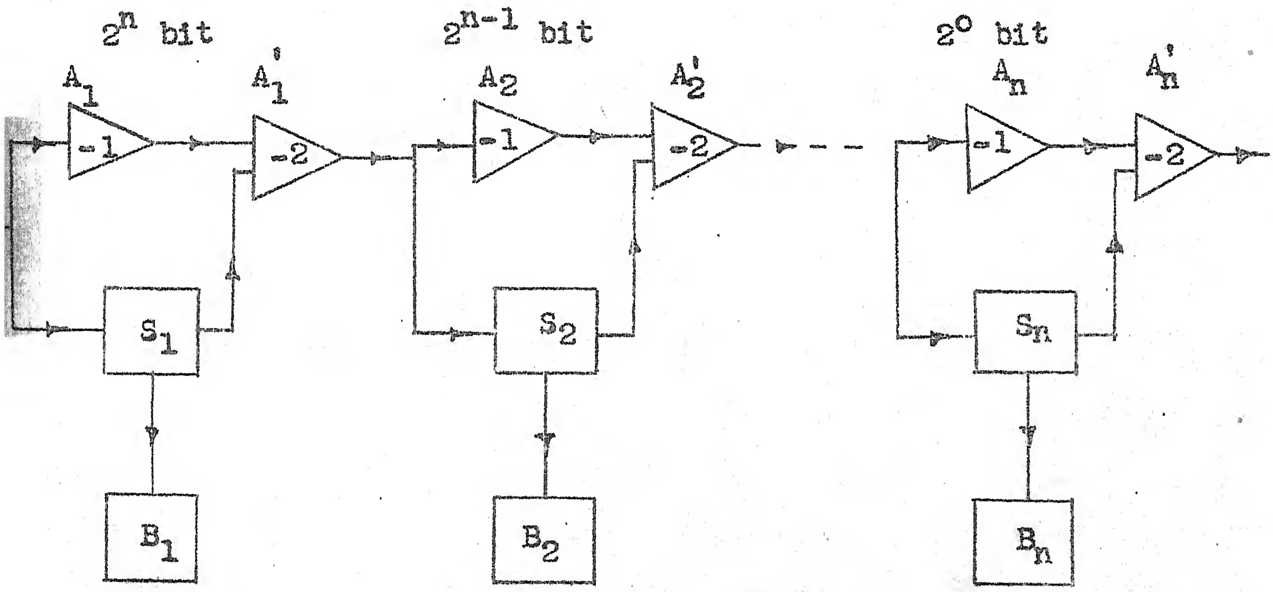


FIG. 9. BASIC BLOCK DIAGRAM OF THE SCHEME.

information in the digital form and display it by means of neon bulbs.

Assuming that each unit operates instantaneously, the operation of the system can be described in brief as follows: The incoming voltage is compared with threshold voltage x. If it is larger than the threshold then the threshold device gives output '1' by changing its output voltage level by x volts. If the input is less than x volts, the Schmitt trigger output is '0' and there is no change in its output voltage level. The same incoming input is also applied to the inverter A. The output of the inverter and the Schmitt trigger are added algebraically by the amplifier A', having gain of -2. A factor of 2 is introduced here to make the following stages identical to the first stage thus reducing the design problem. The whole operation can be described by saying that the single unit of A/D converter having an input output relationship given by the eqn. (2.1) and eqn. (2.2) and depicted in the Figure 10.

$$\left.\begin{aligned} D_n &= 0 \quad \text{for} \quad V_n \quad x \\ &= 1 \quad \text{for} \quad V_n \quad x \end{aligned}\right\} \qquad \text{---} \quad (2.1)$$

$$V_{n+1} = 2\,(V_n - x \cdot D_n) \qquad \text{---} \quad (2.2)$$

where n refers to the stage number

D_n is the binary output of the nth stage

V_n is the input voltage to the nth stage

V_{n+1} is the output of the nth stage and input to $(n+1)^{th}$ stage.

The first transfer function equation (2.1), specifies the desired relation between the digit output D_n and the input V_n. D_n is zero when V_n is below the reference voltage x and $D_n = 1$ when V_n is above the threshold voltage x. The second transfer

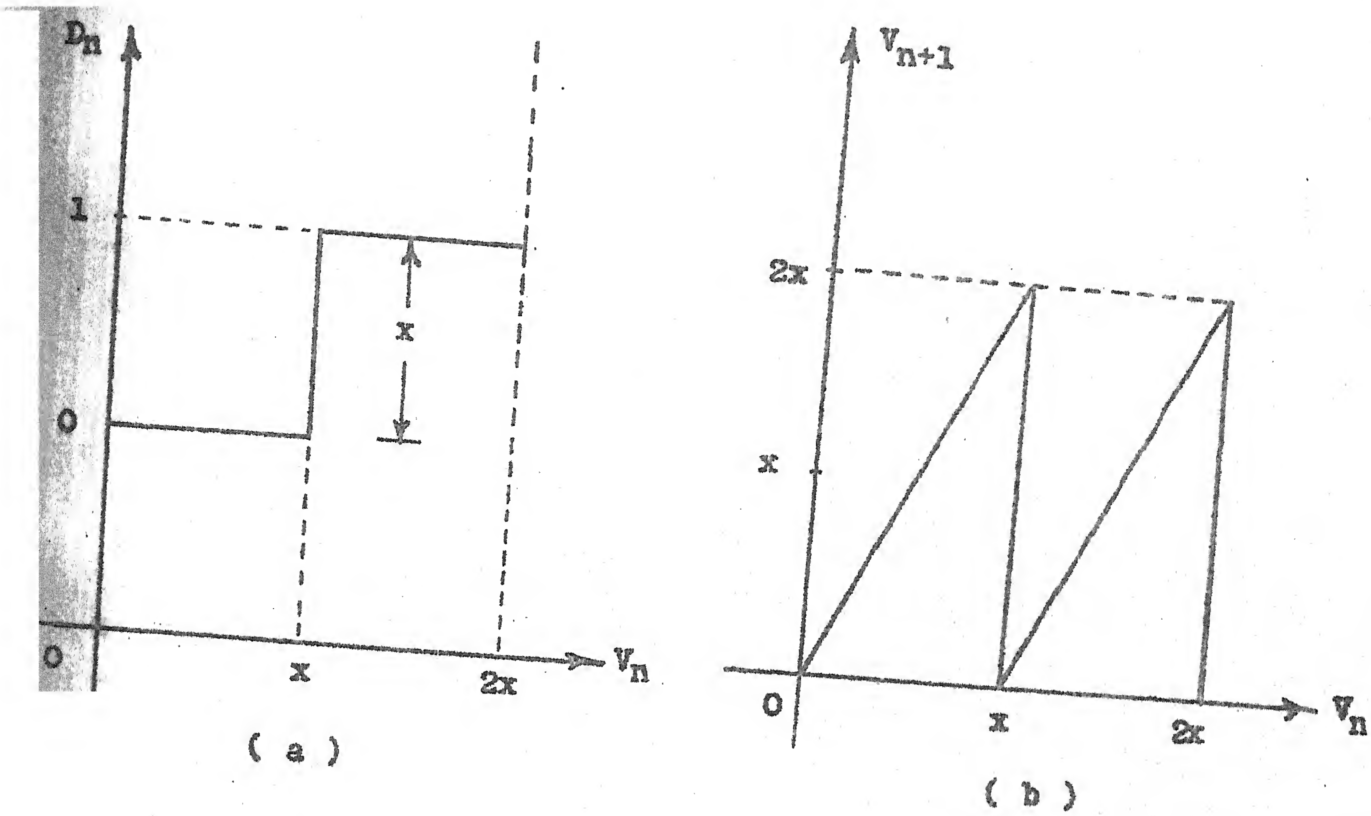


FIG. 10. TRANSFER FUNCTION

function shows the relation between the input to the n^{th} stage V_n and its output V_{n+1}. If V_n is less than threshold there is no subtraction operation. The input itself gets doubled and is fed to the next stage. Otherwise $D_n = 1$ and the difference of input and the threshold device output is doubled and fed as input to the $(n+1)^{th}$ stage. This transfer function is given by eqn. (2.2). Thus the gain of two is necessary in the adding amplifier only when the reference voltage of the following stages is to be kept x volts. However, it may be mentioned that if the threshold value of the successive stages could be adjusted to x/2, x/4, ... etc., then there will be no need of having a gain of -2 in the summing amplifier.

The theoretical assumption that all the units in the basic block diagram (Fig. 9) operate instantaneously is not valid for, in practice, there is some delay involved in the operation of the Schmitt triggers due to the finite rise time of the input pulse. Thus, for inputs greater than x, i.e., 8 volts, the stage output initially begins to rise to twice the input pulse amplitude (Fig.11). The Schmitt then triggers reducing the stage output to its final value which is twice the difference between the input voltage and the Schmitt's output. Similarly, at the termination of the pulse (back edge), when Schmitt changes back to its ground state there is still some input to the Amplifier A' due to the finite fall time of the sample pulse. Hence there are spikes in the leading and trailing edges of the resultant waveform which is amplified by the Summing Amplifier A', (Fig. 11).

Savitt[4] considers that the minimisation of hysteresis

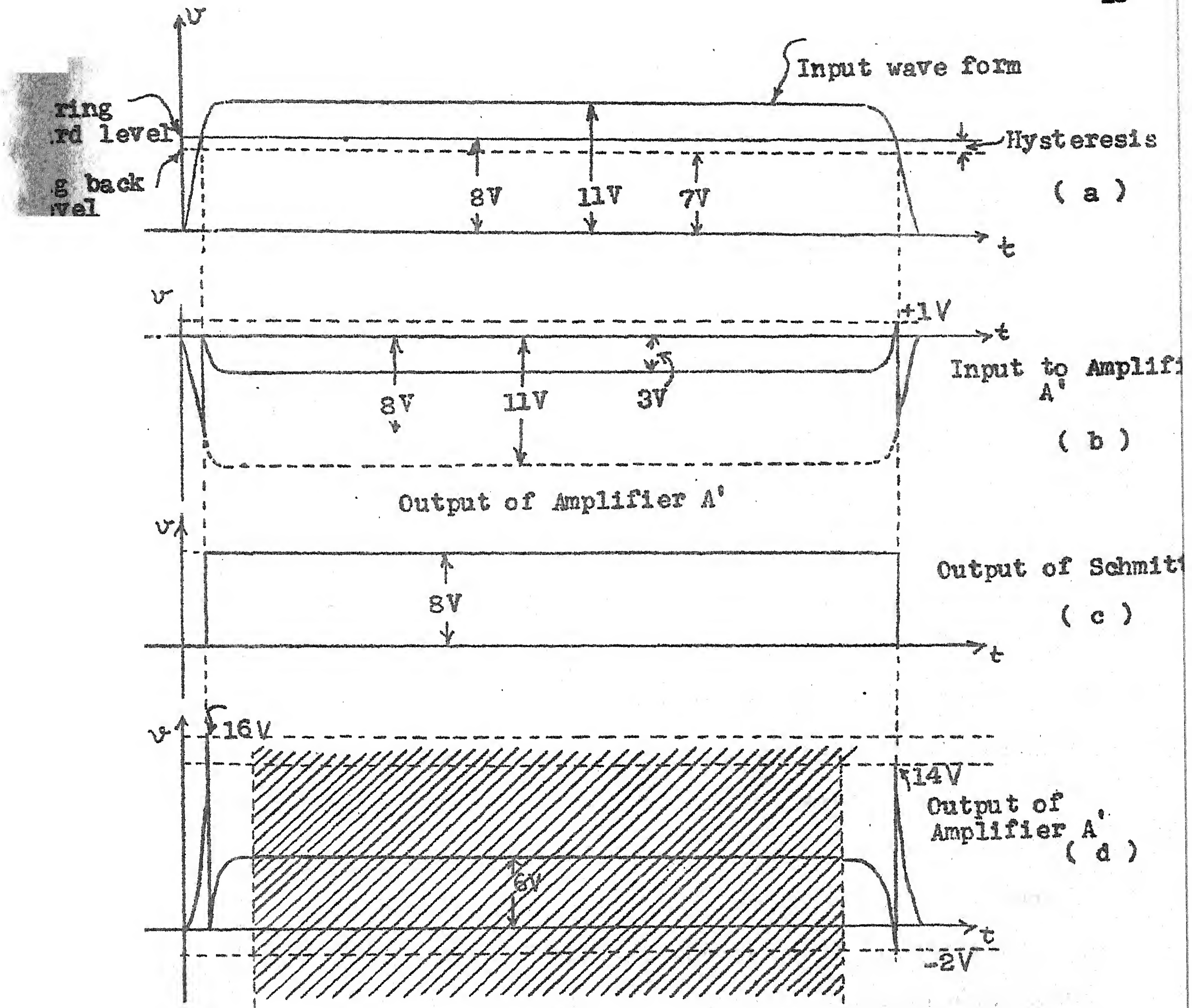


FIG. 11. EFFECT OF DELAY IN THE OPERATION OF SCHMITT TRIGGER.

in the Schmitt circuit will eliminate the problems arising from these spikes. Reduction of hysteresis will tend to make the circuit unstable. Thus, for finite hysteresis, little examination would reveal that the propagation of these spikes through successive stages can result in unpredictable and erroneous digital output.

Fig. 11 shows the various waveforms at different points of the circuit when pulses of finite rise times are fed into the Schmitt trigger and amplifier A. The Schmitt triggers are assumed to change state instantaneously. Once again, this is seldom true in practice, for, Schmitt rise times may be comparable to the amplifier rise times. Thus, in general, the prediction of the exact waveforms and the response of the successive stages to these spikes is a difficult task. The insertion of low pass filters to remove the spikes inevitably results in slower rise times for pulse inputs into the successive stages. Hence suitable modifications are called for in order to obtain reliable operation of Savitt's scheme.

A straightforward solution to the problem is to resample the output of each stage of the A/D converter in appropriate time sequence. After sufficient time is allowed for making decisions in a given stage, the output is sampled and fed on to the next stage. This would necessitate the incorporation of a few more blocks in each stage (as shown in Fig. 12) which increases the overall system complexity. The output of amplifier A and the Schmitt trigger are fed to the summing amplifier A' through a signal gate. This signal gate is controlled by a monostable multivibrator which is triggered by the input pulse itself delayed

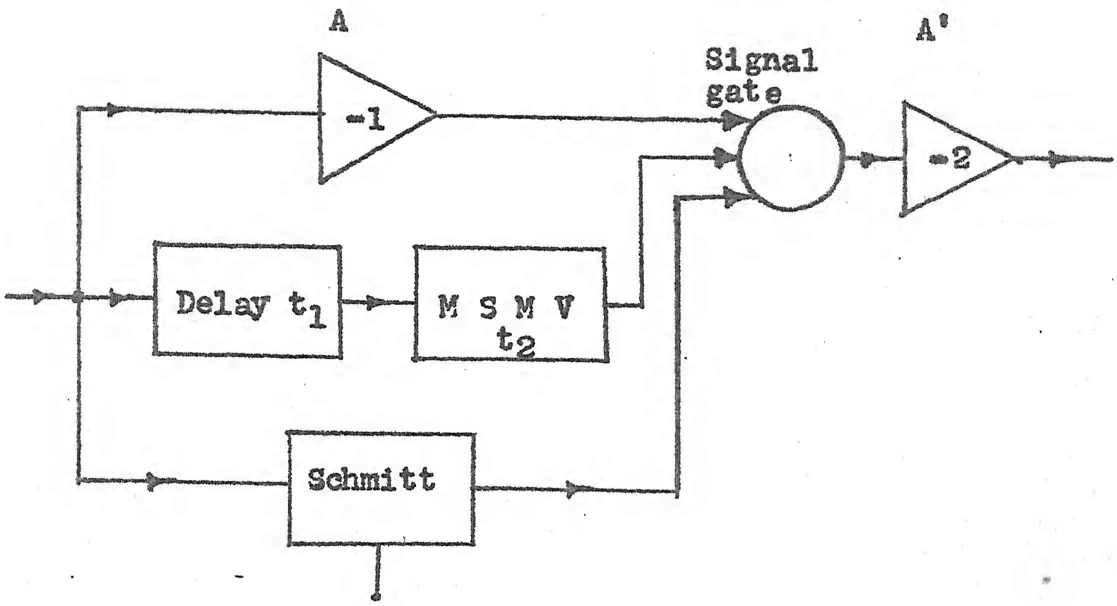


FIG. 12. MODIFIED BLOCK DIAGRAM OF ONE ENCODER STAGE (METHOD I).

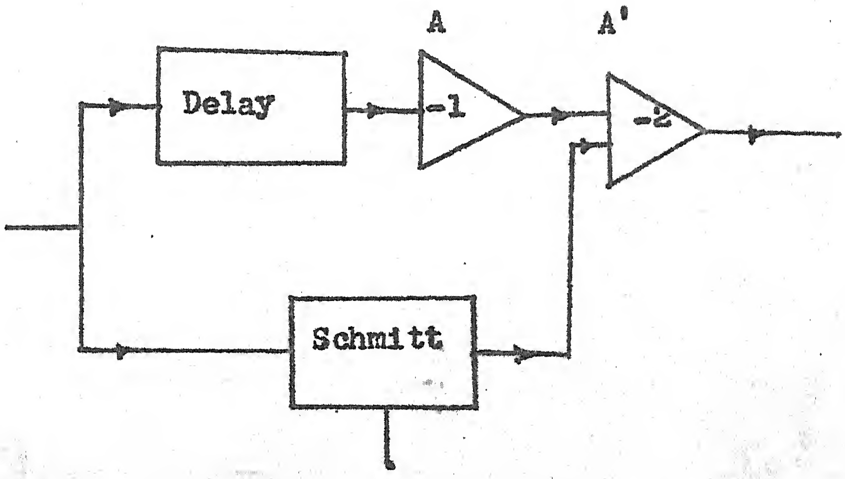


FIG. 13. MODIFIED BLOCK DIAGRAM OF ONE ENCODER STAGE (METHOD II).

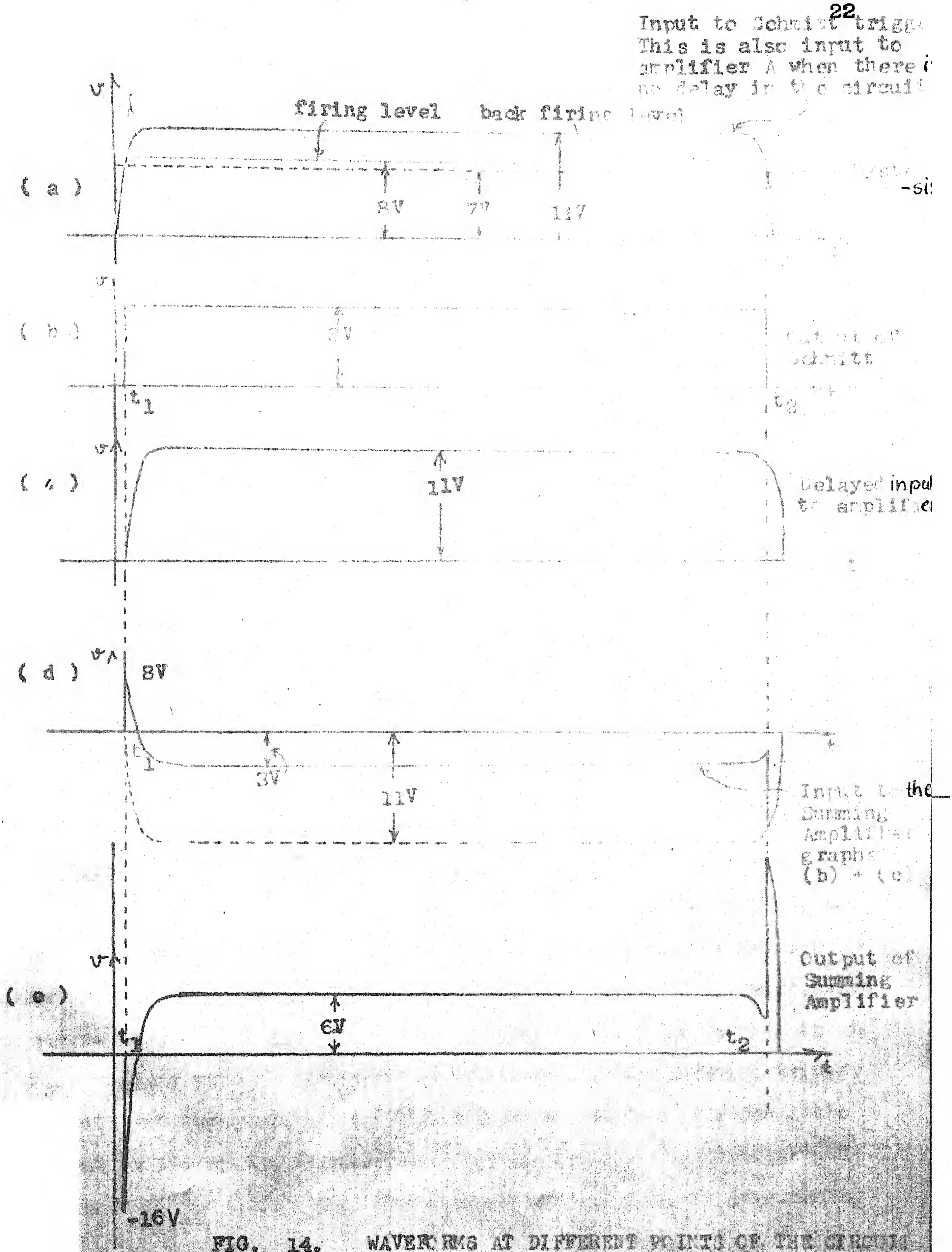


FIG. 14. WAVEFORMS AT DIFFERENT POINTS OF THE CIRCUIT AFTER INTRODUCTION OF DELAY.

through a delay t_1. The monostable multivibrator is adjusted to have the quasi-stable state period equal t_2, the duration for which the output is sampled. The shaded area in Fig. 11.d corresponds to this period. Alternately, the signal gate may be introduced at the output of the amplifier A'. It may be mentioned that with this scheme, the pulse duration of the input to the subsequent encoder stages will reduce successively. This can be taken care of by having a sufficiently wide input pulse into the first stage.

The second method is to introduce a fixed amount of delay in the circuit as shown in Fig. 13, so that the signal is not allowed to reach the summing amplifier before the Schmitt fires. This will, however, result in generation of a negative going spike at the leading edge of the resultant waveform as shown in Fig. 14.e. The instant t_1, at which the Schmitt fires, depends upon the rise time of the input waveform as shown in Fig. 14.a. The maximum delay for the Schmitt occurs when the input has a value slightly greater than 8 volts. Hence the amount of the delay introduced prior to the amplifier A should be made equal to this maximum delay. With the delay introduced, a positive going spike occurs at the trailing edge of the waveform at the instant t_2, the instant when the Schmitt returns to its ground state. The Schmitt triggers of the successive stages might be triggered by these spikes during this period t_2 to t_3. Hence a gate is used between the output of the Schmitt trigger circuit and the input of the binaries to ensure that the Schmitt's output is fed to the respective binaries only for the duration T_1 instead of T_2 (Fig. 15). The opening of this gate is governed by

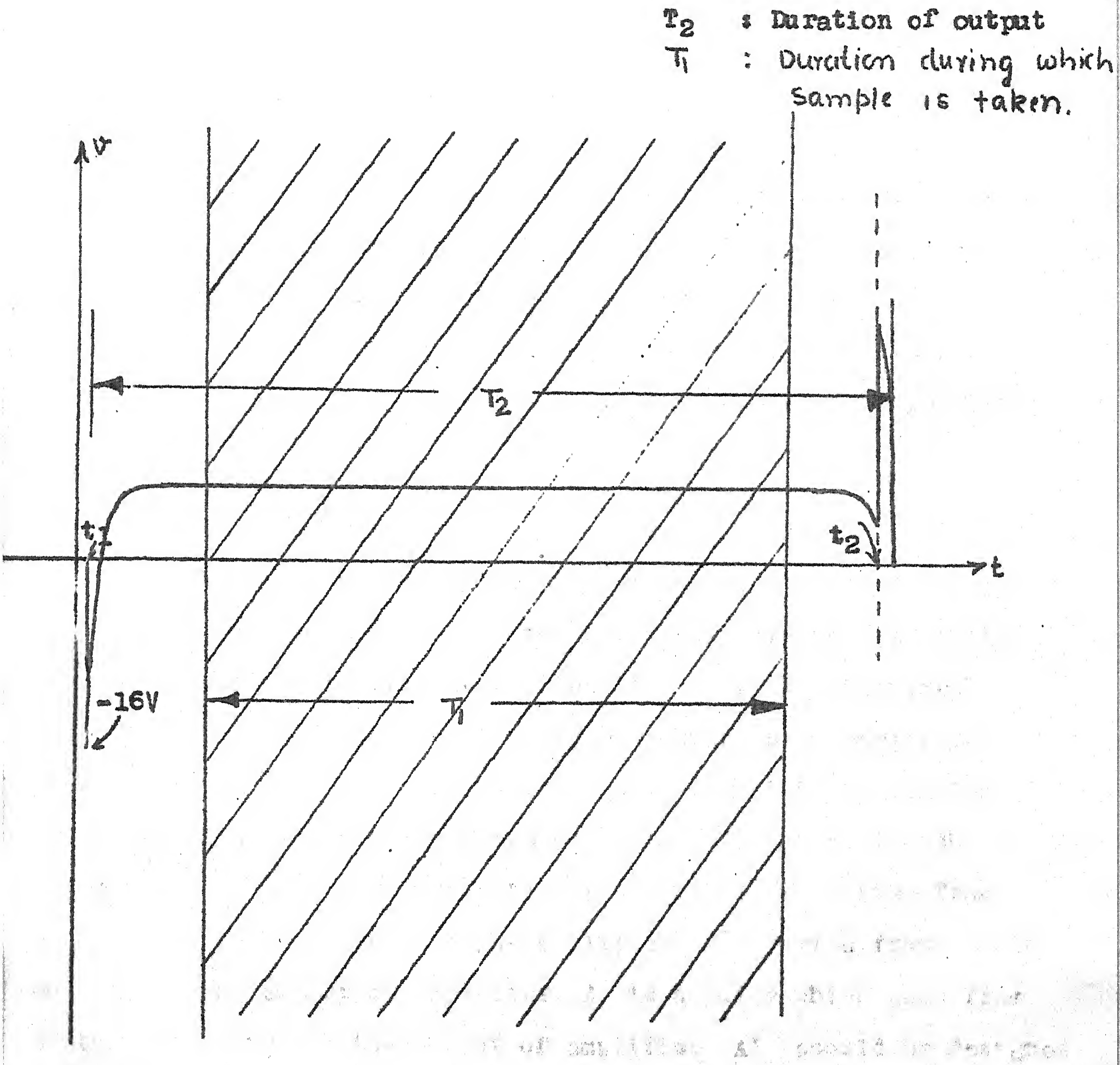


FIG. 15. FIG. 14(d) REPRODUCED. WITH SHADOWED AREA INDICATING THE PERIOD DURING WHICH SCHMITT'S OUTPUT IS ALLOWED TO REACH THE BINARY.

the output of a monostable multivibrator circuit which is a pulse of duration T_1.

Sampling Unit: The scheme of obtaining a sample from the analog voltage input at any desired instant is also shown in Fig. 7. The input is applied to a six diode gate. The controlling voltages for this gate are obtained from a binary which in turn is triggered by a monostable multivibrator. Thus, the duration of the sample pulse can be controlled and the rate of sampling is governed by the rate at which the monostable multivibrator is triggered. This is achieved by the clock input into the monostable multivibrator.

3.2. ENCODER UNIT DESIGN:

3.2.1. The Amplifiers:

Each stage of the A/D converter employs two amplifiers, A and A', with gains of -1 and -2. These amplifiers should have stable gains and excellent linearity . The required stability and linearity are obtained by making use of negative feedback in the design. The maximum input signal to be handled is chosen as 16 volts which fixes the value of Schmitt threshold to be 8 volts. Thus the input to the amplifier A varies from 0 to 16 volts and that of the amplifier A' varies from 0 to -8 volts. The output of amplifier A is a pulse which goes from 0 to -16 volts and the output of amplifier A' should be designed to yield a positive going pulse of 0 to 16 volts. The circuit diagram of the amplifier is shown in Fig. 16.b. It consists of a common emitter stage followed by a common collector stage. Thus the common emitter stages gives the inverting gain and the output impedance is reduced by the emitter follower stage. The configuration

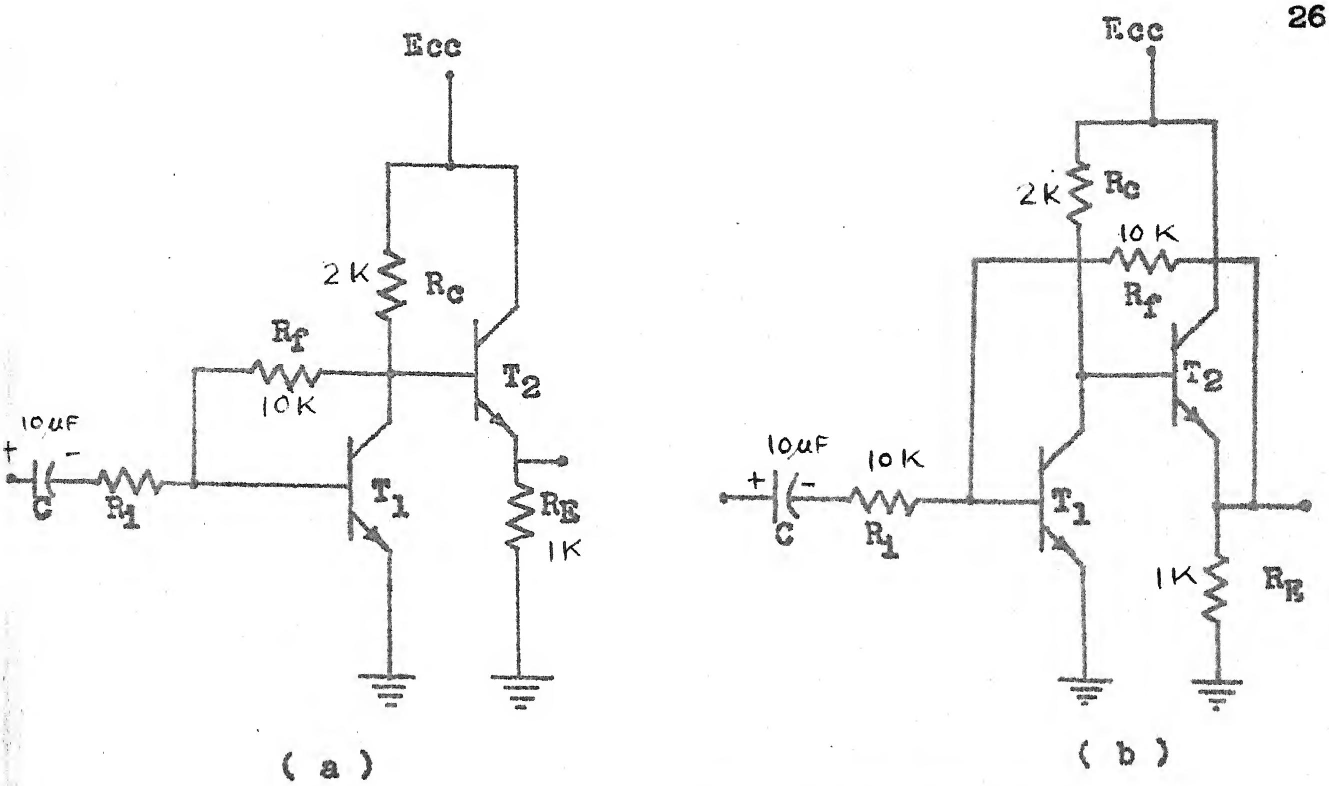
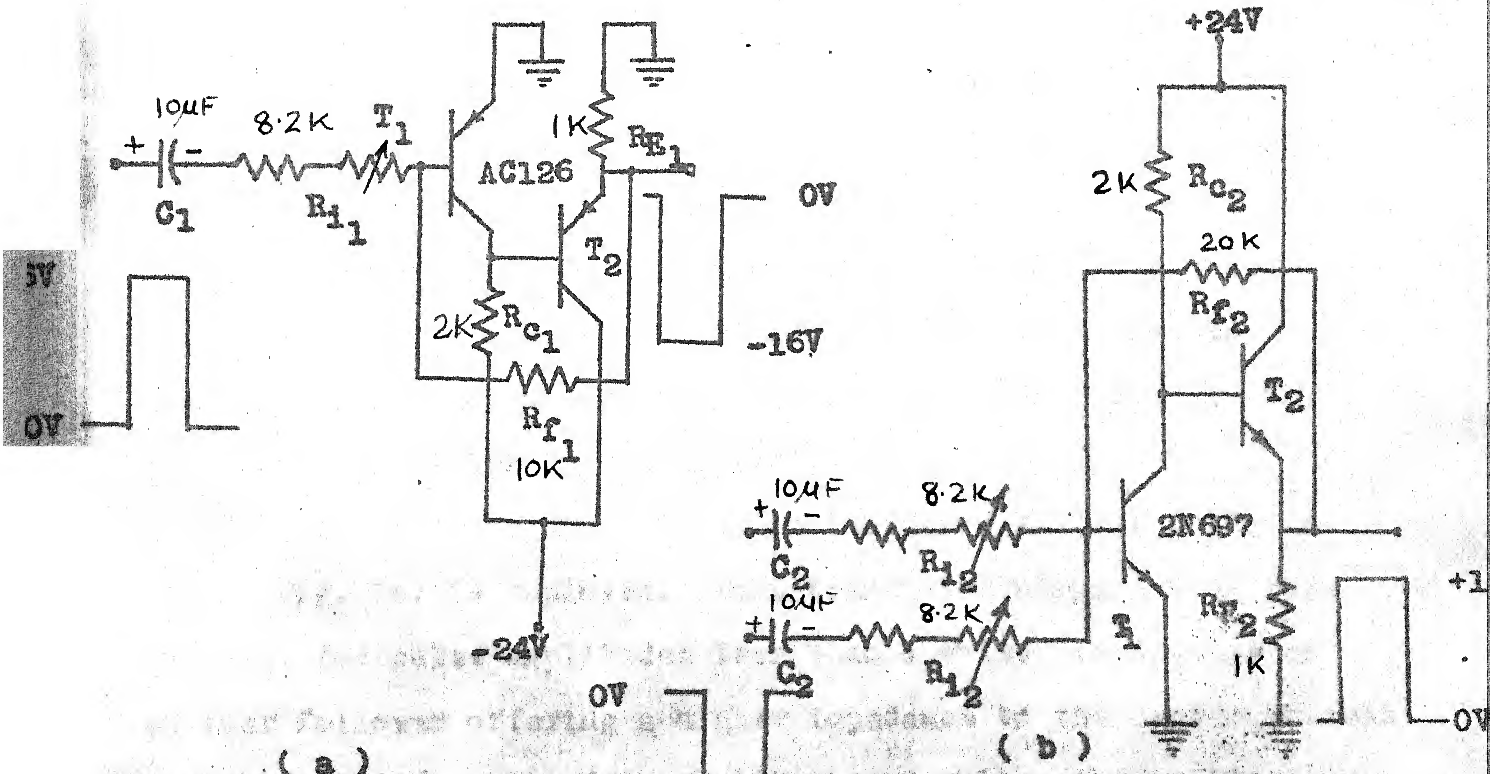


FIG. 16. TWO POSSIBLE WAYS OF PROVIDING FEEDBACK.



(a)
Amplifier A with gain -1

(b)
Amplifier A' with gain -2

FIG. 17. COMPLEMENTARY CONFIGURATIONS OF AMPLIFIER A AND A'.

shown in Fig. 16.b is preferred as the overall feedback tends to stabilize the d-c conditions as well. Also the output impedance is further reduced by the feedback factor. Since the open loop gain of the amplifier is finite (Appendix A) and the resistors used have tolerance of 5%, potentiometers are introduced at the input of each amplifier to adjust the gains. p n p transistors are used for amplifiers with gain -1 and complimentary transistors are used to handle the negative input pulses of the amplifiers with gain -2 (Fig. 17). The detailed analysis of d-c bias conditions and signal performance of the amplifiers are given in Appendix A_1- A_3.

3.2.2. Schmitt Triggers:

The Schmitt circuit is designed to have a threshold as well as output of 8 volts. The various components chosen are as shown in Fig. 18. Potentiometer P_1 controls the output voltage swing by controlling the current through R_{c2} whereas potentiometer P_2 controls the threshold voltage. If the input to the Schmitt trigger circuit is allowed to go up to 16 volts, the transistor T_1 gets saturated offering a low impedance to the pulse source. This non-linear loading of the pulse source combined with the finite output impedance of the source affects the input going into the inverting amplifier A.

In order to avoid this, an isolating emitter follower (T_3 in Fig. 18) is employed. This transistor plays a dual role in that, for pulse amplitudes less than 9 volts, it acts as an emitter follower offering a higher impedance to the source whereas for input pulse amplitudes greater than 9 volts, the emitter-base

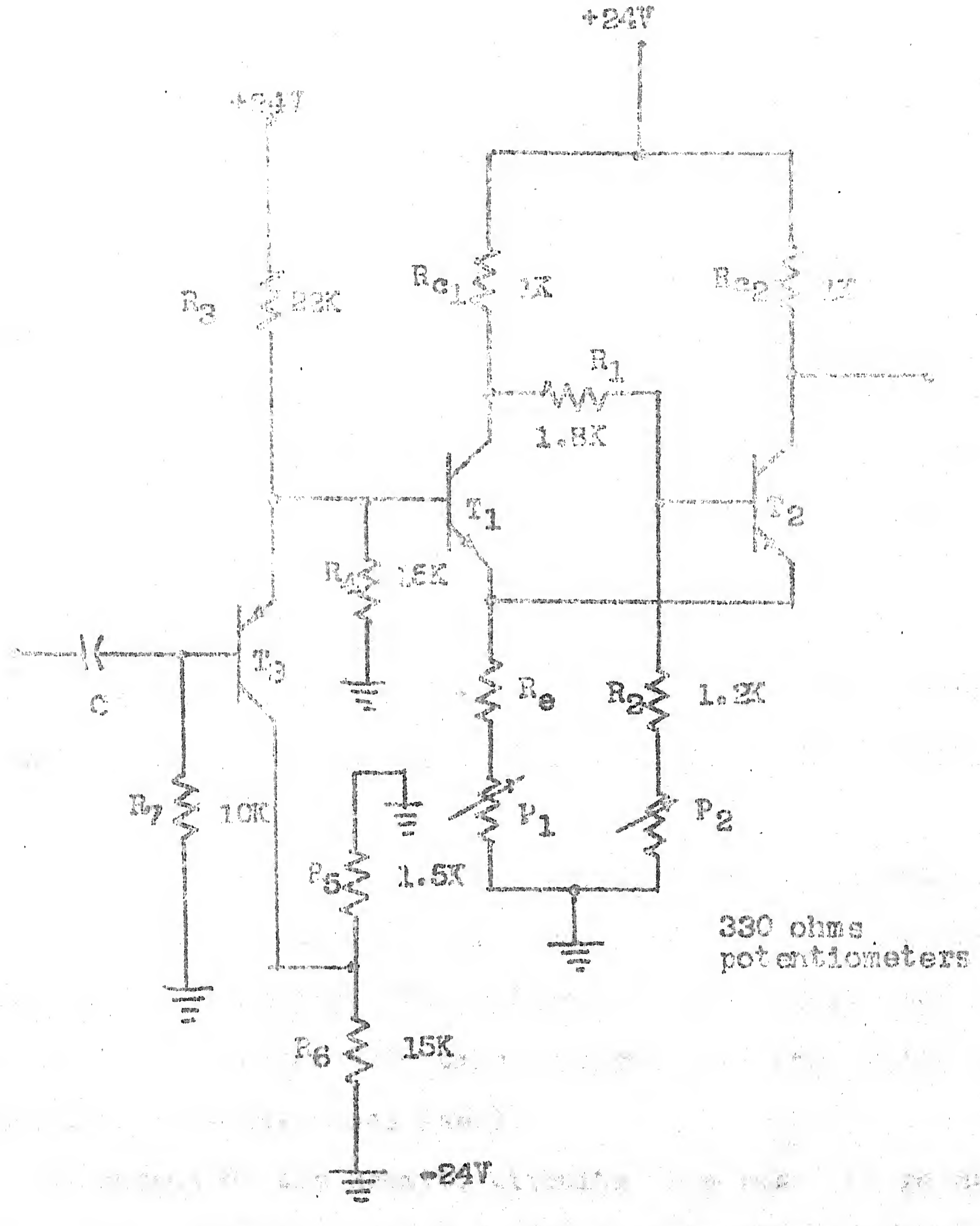


FIG. 18. SCHMITT CIRCUIT WITH ASSOCIATED
INPUT LIMITING CIRCUIT.

junction is reverse biased, thus isolating the source from the Schmitt circuit. Under these conditions, the emitter potential of the transistor T_3 is adjusted to be approximately 9 volts by the proper choice of resistors R_3 and R_4. Such an arrangement prevents the transistor T_1 from saturating which results in an improved performance of the Schmitt from the point of view of speed during the 'switching back' operation. Analysis of this circuit along with the various checks is given in Appendix A_4.

3.2.3. The Storage Unit:

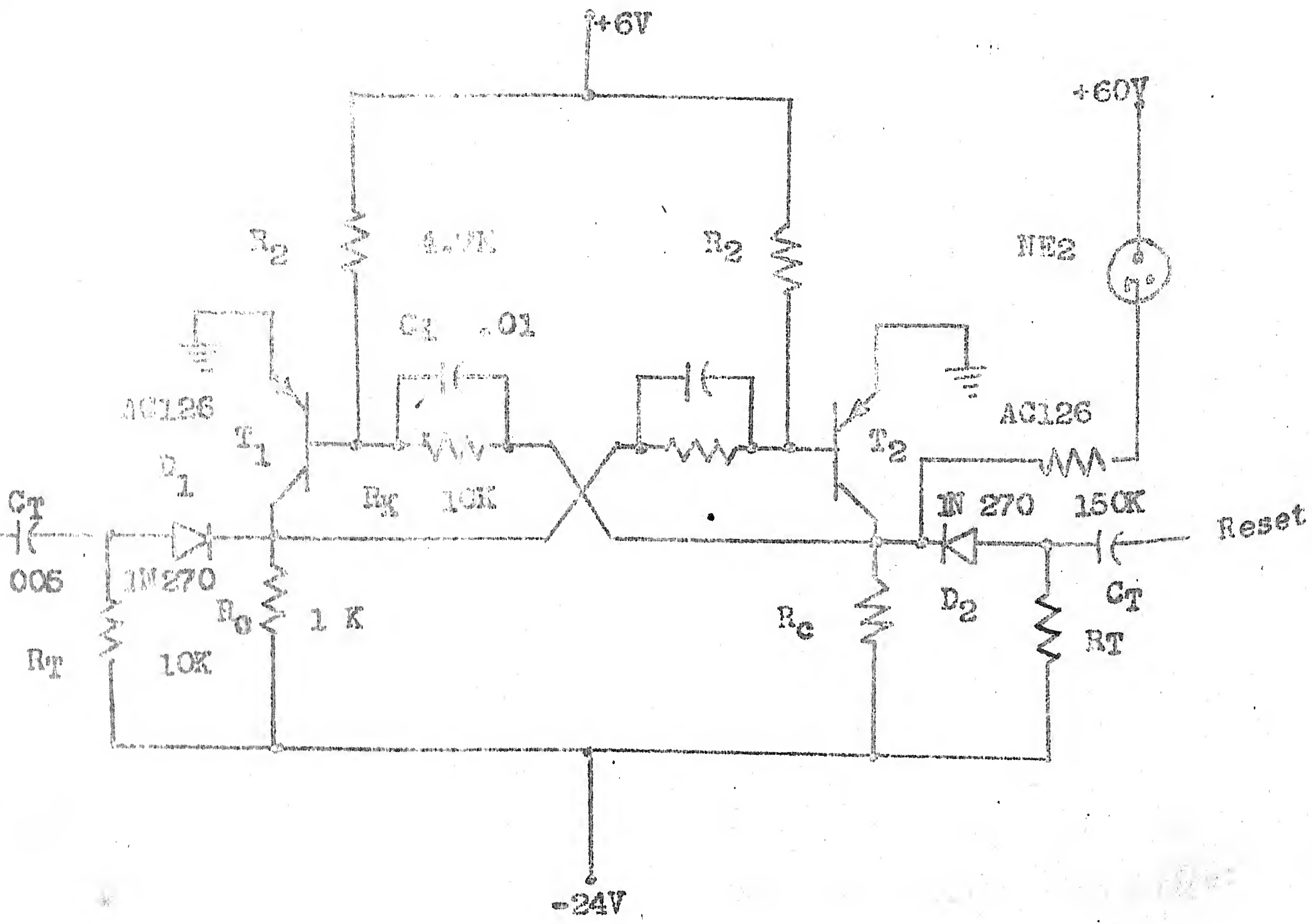
This consists of the binary together with a neon indicator for visual display of its two states. The circuit diagram of the binary is shown in Fig. 19.

Positive pulses applied through diode gates achieve the operations of setting and resetting the binary. The diode gates prevent any false triggering due to the back edge of the input pulse.

In the ground state of the binary (on the application of the reset pulse) transistor T_1 is turned off and T_2 goes into conduction and is saturated. The collector potential of T_2 is approximately zero and the neon bulb is turned off (60 volts is not enough to strike the neons used).

The output of the Schmitt circuits is a positive going step of 8 volts. This is applied to the 'set terminal' of the binary which causes a change in state (transistor T_2 is biased off and T_1 goes into conduction). The collector voltage of the transistor T_2 tends to B^- (-24 volts) which causes the neon bulb to strike thus registering a digital output.

The design details of the binary are given in Appendix A_5.



All capacitors are in micro-farads.

FIG. 19. BINARY CIRCUIT.

3.2.4. The Gating Circuit:

The gating circuit is interposed between the Schmitt trigger and the storage unit. Its function is to allow the output of the Schmitt to reach the binary only for 600 micro-secs, so that in the vicinity of the training edge of the sample input pulse (1 millisecond), the Schmitts are not able to transfer any information to the registering unit.

The gating circuit consists of a transistor gate (Fig. 20) whose controlling pulse is derived from a monostable multivibrator (Fig. 21). The gate circuit consists of a single ended chopper circuit using a transistor. On the arrival of a negative pulse at the base of the transistor, it is turned off and the output terminal assumes the signal potential. When the pulse is removed the transistor is saturated by the bias current through R_b, thus keeping the output short circuited to ground.

The monostable multivibrator is shown in Fig. 21. The triggering pulse is obtained from the Schmitt trigger. The output is a negative going pulse of 600 micro-secs duration which is fed to the base of the gating transistor.

3.3. THE SAMPLING UNIT:

The sampling unit consists of a six diode sampling gate[5] whose control voltages are obtained from a binary. The triggering pulse of the binary is obtained from a monostable multivibrator having an output time period of 1 millisecond. Since the signal is always positive going (0 to +16 volts) the control voltages of the sampler are chosen to be -4 volts and +20 volts. The various

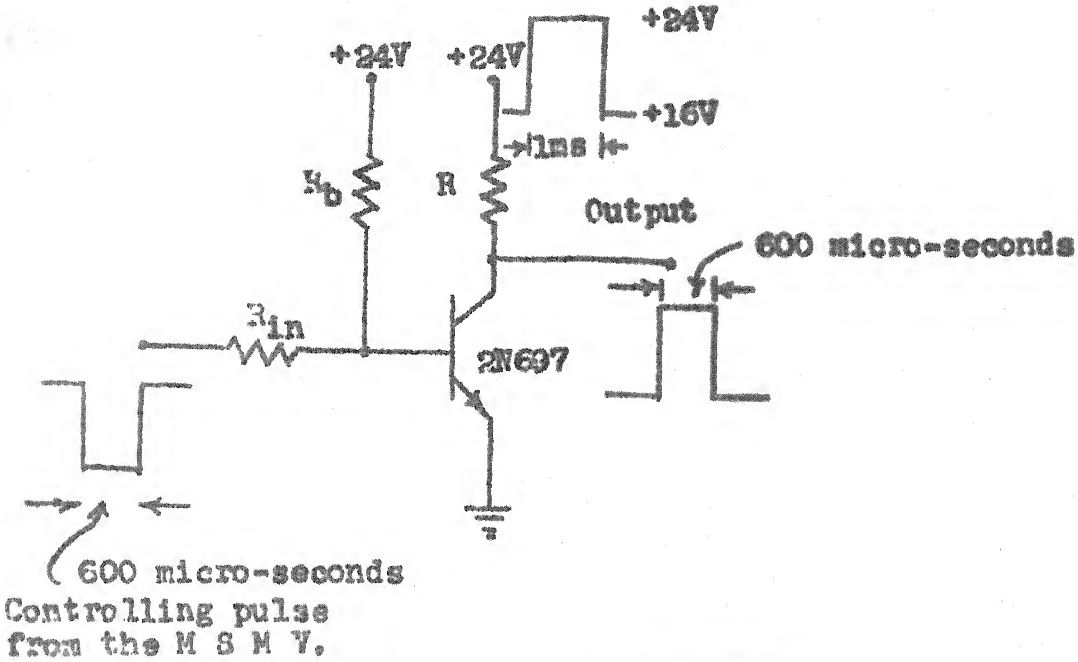


FIG. 20. TRANSISTOR GATE CIRCUIT.

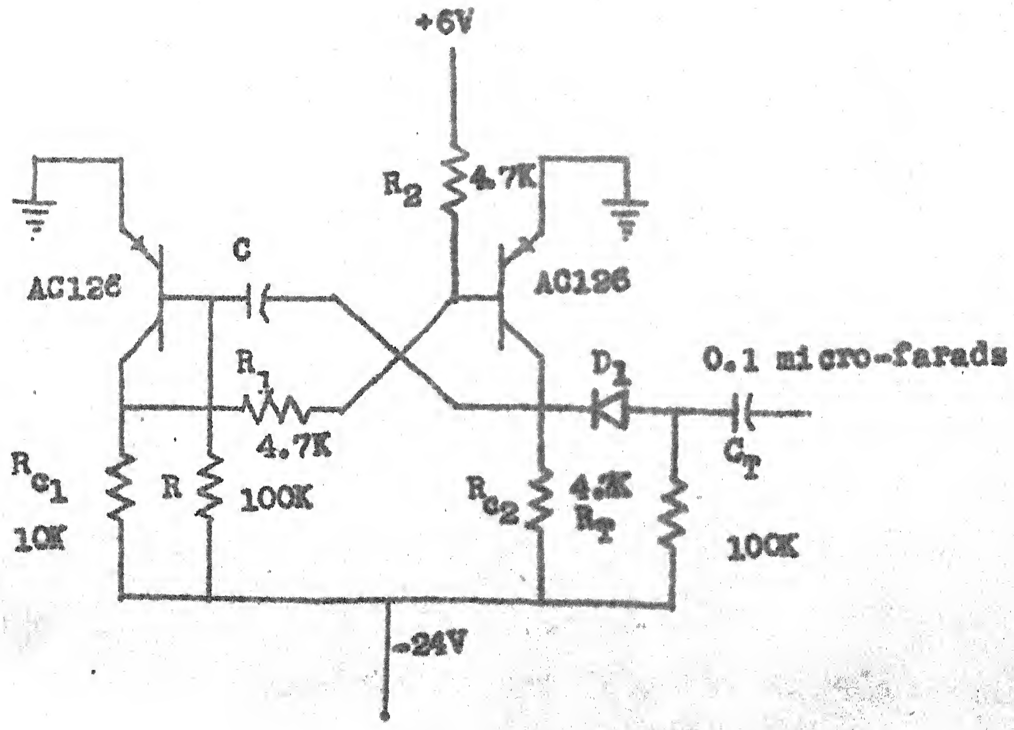
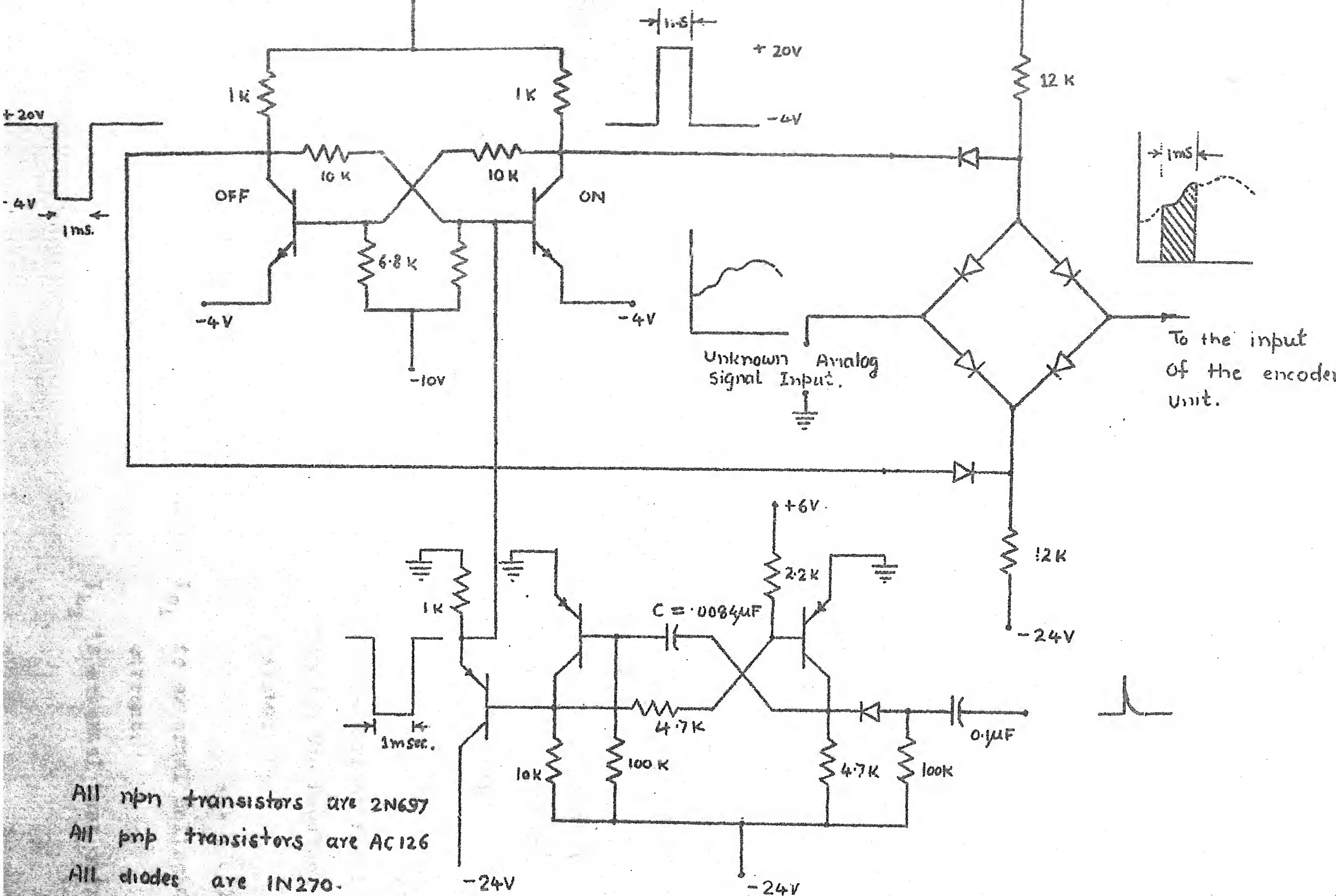


FIG. 21. MONOSTABLE MULTIVIBRATOR CIRCUIT.

component values of the six diode sampler, binary and the monostable multivibrator are as shown in Fig. 22. The design considerations are given in the Appendix A_7.



All npn transistors are 2N697
All pnp transistors are AC126
All diodes are IN270.

Fig Various units of Sampling Unit.

APPENDIX A

A_1 - The feedback amplifiers:

The calculation of the quiescent operating potential (E_o) of the feedback amplifier is done as follows. Consider the circuit shown in Fig. 23. Subscripts 1 and 2 pertain to transistors T_1 and T_2 respectively. The symbols α, β, I_{co_1} and I_{co_2} have usual meanings.

The d.c. output voltage E_o of the amplifier is given by

$E_o = V_1 - \Delta V$ where V_1 is the d.c. collector potential and ΔV is the base to emitter voltage drop.

$$= B^+ - I_{L_1} R_{c_1} - \Delta V \quad \ldots \quad (A1.1)$$

where B^+ is the supply voltage

I_{L_1} is the load current of transistor T_1

R_{c_1} is the collector load resistance of transistor T_1.

The external base current of transistor T_1 (I_{b_1}) is given by

$$I_{b_1} = I_F = (E_o - \Delta V)/R_F \quad \ldots \quad (A1.2)$$

where I_F is the current flowing through the feedback resistor R_F.

$$I_{L_1} = I_{c_1} + I_{b_2} \quad \ldots \quad (A1.3)$$

where I_{c_1} is external collector current.

I_{b_2} is external base current.

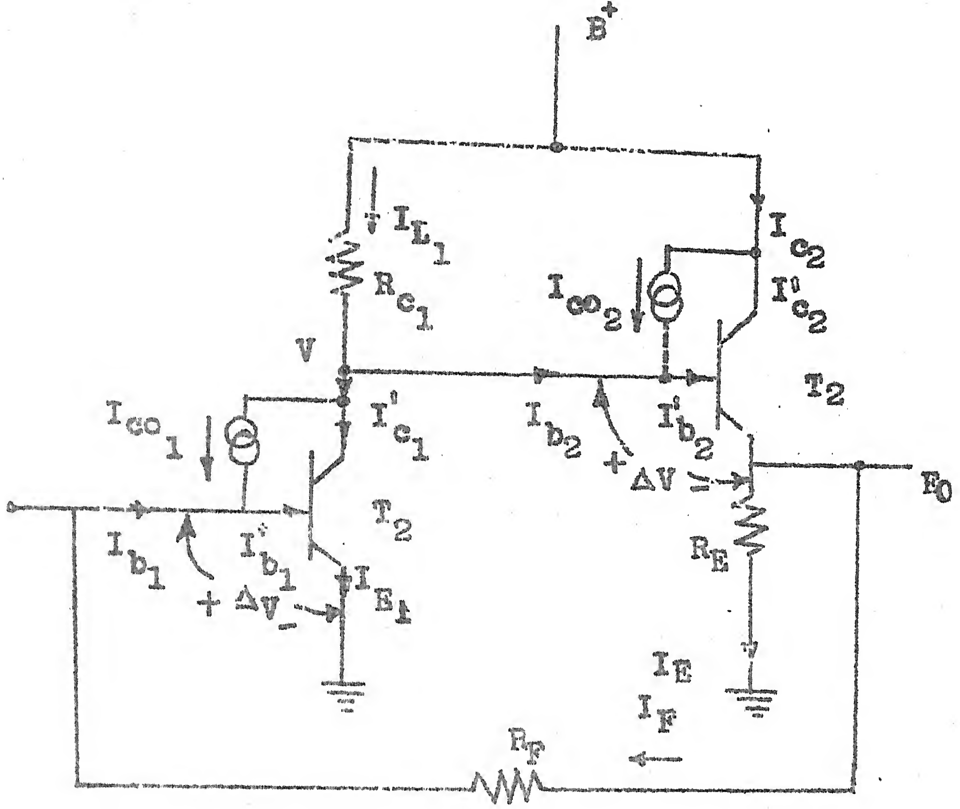


FIG. 23. FEED BACK AMPLIFIER CIRCUIT

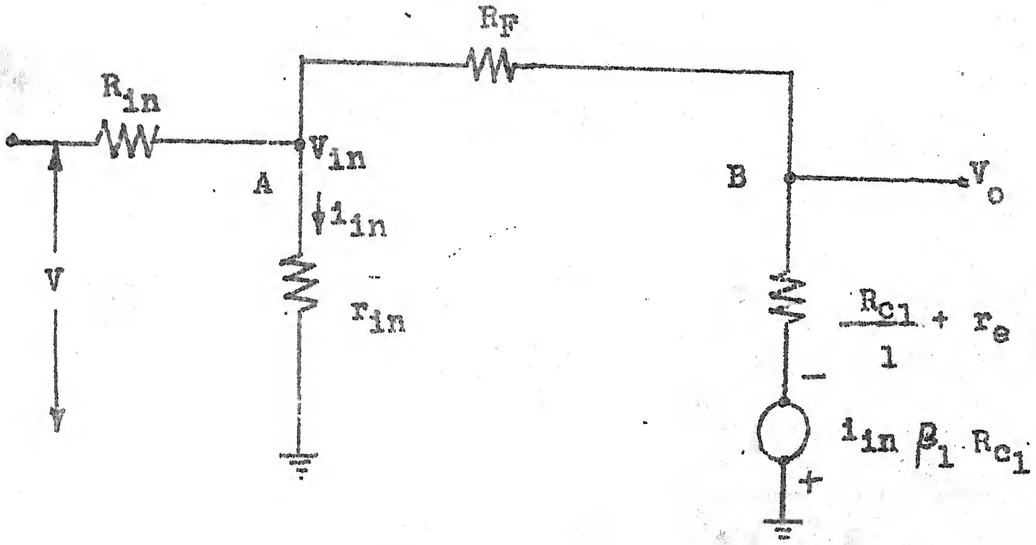


FIG. 24. SMALL SIGNAL MODEL OF THE FEEDBACK AMPLIFIER.

$$I_{c_1} = I_{co_1} + I_{b_2}$$

$$= I_{co_1}(\beta_1 + 1) + \frac{(E_o - V)}{R_F}\beta_1 \qquad \ldots \qquad (A1.4)$$

The external base current of transistor T_2 is given by

$$I_{b_2} = I'_{b_2} - I_{co_2} \qquad \ldots \qquad (A1.5)$$

where I'_{b_2} is the base current of leakage free 'inner' transistor T_2.

$$= \frac{\alpha_2}{\beta_2}\left(\frac{E_o}{R_E} + \frac{E_o - \Delta V}{R_F}\right) - I_{co_2} \qquad \ldots \qquad (A1.6)$$

where R_E is the bias resistance of the emitter follower.

From the above equations

$$E_o = \frac{B^+\left[1 - \frac{\Delta V}{B^+}\left\{1 - \frac{R_{c_1}}{R_F}(\beta_1 + 1)\right\} - \frac{I_{co_1}}{B^+}R_{c_1}(\beta_1 + 1) + \frac{I_{co_2}R_{c_1}}{B^+}\right]}{1 + \frac{R_{c_1}}{R_F}\left(\beta_1 + \frac{\alpha_2}{\beta_2}\right) + \frac{R_{c_1}}{R_E}\frac{\alpha_2}{\beta_2}} \qquad \ldots \qquad (A1.7)$$

If I_{co_1} and I_{co_2} are such that the terms containing I_{co_1} and I_{co_2} are negligible as compared to the other terms in the numerator,

$$E_o = \frac{B^+\left[1 - \frac{\Delta V}{B^+}\left\{1 - \frac{R_{c_1}}{R_F}(\beta_1 + 1)\right\}\right]}{1 + \frac{R_{c_1}}{R_F}\left(\beta_1 + \frac{\alpha_2}{\beta_2}\right) + \frac{R_{c_1}}{R_E}\frac{\alpha_2}{\beta_2}} \qquad \ldots \qquad (A1.8)$$

Transistors type AC126 (Germanium - p n p) and type 2N697 (Silicon - n p n) were chosen for the amplifier A of gain -1 and amplifier A' of gain -2 respectively. The pertinent specifications

are as shown in Table A1.1.

In amplifier A with B^+ 24V , R_{c_1} 2K , R_E 1K , R_F 10K ; E_o = 0.52V from eqn. (A1.7). Hence emitter current of transistor T_1 (I_{E_1}) is given by

$$I_{E_1} = 11.8 \text{ mA} \qquad \ldots \qquad (A1.9)$$

In amplifier A' with B^- -24V , R_{c_1} 2K , R_E 1K , R_F 20K ; E_o = 3.6V from eqn. (A1.8). Hence emitter current of transistor T_1 (I'_{E_1}) is given by

$$I'_{E_1} = 10.2 \text{ mA} \qquad \ldots \qquad (A1.10)$$

Transistor type	Max. dissipation	I_{CB_o}	BV_{CB_o}	BV_{EB_o}	BC_{CE_o}	β	V
AC126	500 mw	200µA	32V	10V	32V	50	0.2V
2N697	600 mw	1µA	60V	5V	40V	50	0.6V

TABLE A1.1 Transistor specifications

A_2 - Small signal model of the feedback amplifier:

Consider the circuit shown in Fig. 24. It is the small signal model of the feedback amplifier as shown in Fig. 16 b. with the assumptions that $\frac{R_e}{\beta_2} + \frac{r_b}{\beta_2} + r_e$ is very less as compared to R_E ; $\frac{R_e}{\beta_2}$ and r_e are very large as compared to $\frac{r_b}{\beta_2}$. Current i_{in} going into the base of transistor T_1 causes a potential change of

$i_{in}\beta_1 R_{c_1}$ at the collector of T_1. The same voltage change appears at the emitter of T_2. This is shown in Fig. 24 by the voltage generator E.

Consider the node equation at the node A.

$$\frac{V - V_{in}}{R_{in}} = \frac{V_{in}}{r_{in}} + \frac{V_{in} - V_o}{R_F} \qquad \ldots \qquad (A2.1)$$

$$V_o = -\frac{V_{in}}{r_{in}}\beta_1 R_{c_1} + \left(\frac{V_{in} - V_o}{R_F}\right) R_o \qquad \ldots \qquad (A2.2)$$

From eqns. (A2.2) we get

$$V_o = V_{in}\frac{\left(\frac{R_o}{R_F} - G\right)}{\left(\frac{R_o}{R_F} + 1\right)} \qquad \text{where} \quad G = \frac{\beta_1 R_{c_1}}{r_{in}}$$

$$R_o = \frac{R_{c_1}}{\beta_2} + r_e$$

If $G \gg 1 \gg \frac{R_o}{R_F}$, we have

$$V_o \approx -G\, V_{in} \qquad \ldots \qquad (A2.3)$$

Substituting V_{in} from eqn. (A2.3) in the eqn. (A2.1), we get

$$\frac{V_o}{V} = -\frac{1}{\frac{R_{in}}{G\, r_{in}} + \frac{1}{G} + \frac{R_{in}}{R_F G} + \frac{R_{in}}{R_F}} \qquad \ldots \qquad (A2.4)$$

$$\frac{V_o}{V} = -\frac{1}{\frac{1}{G}\left\{\frac{R_{in}}{r_{in}} + 1\right\} + \frac{R_{in}}{R_F}\left\{\frac{1}{G} + 1\right\}} \qquad \ldots \qquad (A2.5)$$

From eqn. (A2.5), if $G \gg \frac{R_{in}}{r_{in}}$, we have

$$\frac{V_o}{V} \approx - \frac{R_F}{R_{in}} \qquad \ldots \qquad (A2.6)$$

In the desing of the amplifiers $G_{min} \approx 200$, $\frac{R_{in}}{r_{in}} \approx 20.$

A_3 - Open loop small signal gain (G):

$$G \approx \frac{\beta'}{h_{ie}} R_{c_1} \qquad \ldots \qquad (A3.1)$$

where h_{ie} is the a-c input resistance of transistor.

R_{c_1} is the load resistance.

Since $h_{ie} = \beta' r_e + r_b$ and if $r_b \ll \beta' \cdot r_e$

$$h_{ie} \approx \beta' \left\{ \frac{V^*_T}{I_E} \right\} \qquad \ldots \qquad (A3.2)$$

where β' is the base to emitter current gain for small signals.

r_e is the emitter resistance.

$$V^*_T = n\, V_T \qquad \ldots \qquad (A3.3)$$

where n is 1.5 to 2 for Silicon and 1 for Germanium.

$$V_T = \frac{KT}{q} \qquad \ldots \qquad (A3.4)$$

where K is Boltzmann's constant ($1.38 \; 10^{-23}$ J/ °K)

T is temperature in ^oK

q is electronic charge (1.60 10^{-19}) C.

At room temperature V_T has a value of 26 mV for Germanium and 40 to 50 mV for Silicon.

Open loop small signal gain for amplifier A is 590 from eqns. (A1.9) and (A3.1). It is 260 for amplifier A' from eqns. (A1.10) and (A3.1).

The experimental values of rise and fall times of input and output waveforms of amplifiers A and A' are as shown in Table A3.1.

	Rise time		Fall time	
	Input Waveform	Output Waveform	Input Waveform	Output Waveform
Amplifier A	0.5 μsec	2 μsec	0.5 μsec	2 μ sec
Amplifier A'	0.5 μsec	1 μsec	0.5 μsec	0.5 μsec

TABLE A3.1 The Rise and Fall times of amplifiers A and A'

A_4 - The Schmitt circuit:

The various component values of the Schmitt circuit are as shown in Fig. 18. The base potential of the transistor T_2 is 8.46 volts with the full resistance of potentiometer P_2 in the circuit and is 7.2 volts with the resistance of potentiometer P_2 reduced to zero value. Hence potentiometer P_2 can be adjusted to fix threshold of the Schmitt trigger at 8 volts. The collector current (Ic_2 min) of transistor T_2 with potentiometer P_1

adjusted to its maximum value is 6.32 mA and with P_1 adjusted to its minimum value the collector current (I_{c_2} max) is 8.76 mA. Hence by proper adjustment of the potentiometer P_1, the output current of transistor T_2 can be adjusted to 8 mA giving 8 volts output. The potential at which the Schmitt trigger flips back is 7 volts. Thus the hysteresis is about 1V.

The loop gain of the circuit (L.G.) is given by[6]

$$\text{L.G.} = \frac{gm' \, R_{c_1} \, R_2}{R_1 + R_2 + R_{c_1}} \simeq 8$$

This loop gain is sufficient for the satisfactory operation of the circuit.

A_5 - The Binary:

A saturated flip-flop is designed with supply voltage of 24 volts to obtain an output voltage of 22 volts. The selection of R_1 and R_2 is done so that the following requirements are fulfilled. The 'ON' transistor T_2 must have sufficient base current to saturate it. At the same time emitter-base junction of the transistor T_1 should be reverse biased to ensure that it is cut off in the worst situation. At the same time reverse bias should not exceed the break down voltage (10 volts). The presence of the reverse saturation current (I_{c_o}) tends to bring the 'OFF' transistor into its 'ON' state. This is preferred for keeping the effective base impedance of the 'OFF' transistor low enough so that the drop across it due to I_{c_o} does not exceed the reverse bias of its emitter-base junction. According to these considerations the various component values chosen are as

shown in Fig. 19.

The base current of the 'ON' transistor is about 900 micro-amperes whereas that needed to ensure saturation is 480 micro-amperes. The reverse bias on the 'OFF' transistor is 4.1 volts which keeps T_1 cut off. Effective base resistance of the 'OFF' transistor is 3.3 K ohms. The reverse saturation current being 200 micro-amperes, the effective change in base potential is 0.66 volts for about 10 °C rise in temperature. The emitter-base reverse bias of the 'OFF' transistor being 4.1 volts, with 20° rise in the temperature, the circuit would function satisfactorily.

Steering Circuit:

The steering circuit shown in Fig. 19 comprises of R_T, C_T and diode D_1. R_T must be large enough not to load down the trigger source. At the same time it should be small enough so that any charge which accumulates on C_T during the interval when D_1 conducts will have time to decay during the time between pulses. C_T is trigger coupling capacitor. The time constant should be large enough to provide sufficient triggering drive. Suitable values can be chosen according to the following inequality[7]

$$3\, R_T\, C_T < \tau/2 \quad (\text{where } R_T \gg R_c)$$ and τ is the time period of the incoming pulse.

The function of the commutating capacitor C_K is to assist the binary in making abrupt transitions between its states. The resistor R_K which joins the base of one transistor to the collector of the other and the commutating capacitor should be chosen so that the following inequality is satisfied.

$$3\, R_K\, C_K < \tau$$

Experimental values of these are found to be as $R_T = 10K$, $C_T = 0.005$ micro-farads, $C_K = 0.01$ micro-farads.

Here $3R_K C_K = 0.3$ millisecond

$3R_T C_T = 0.15$ millisecond whereas the input pulse duration $(\tau) = 1$ millisecond.

A_6 - Monostable Multivibrator (M S M V):

The circuit of the MSMV is as shown in Fig. 21. The various design considerations are as follows. The base current of the saturated transistor T_1 should be sufficient to saturate it, i.e., $\frac{E_{bb}}{R} \geqslant (E_{bb} / \beta R_c)$ that is, $R \leq \beta R_c$ which is satisfied for the choice of components shown in Fig. 21. Simultaneously the base-emitter junction of the 'OFF' transistor T_2 should be sufficient to ensure that it remains cut off under the worst conditions. The base potential of T_2 is +4.1 volts whereas the emitter is at ground potential. When the transition takes place, the base current of the transistor T_1 should be sufficient to drive it into saturation, i.e., $\frac{E_{cc}}{R_2} - \frac{E_{bb}}{R_c+R_1} \geqslant \frac{E_{bb}}{R_c}$. With the component values as shown in Fig. 21; $\frac{E_{cc}}{R_2} - \frac{E_{bb}}{R_c+R_1} = 1090$ micro-amperes whereas $\frac{E_{bb}}{R_c}$ is 480 micro-amperes. Hence the above mentioned inequality is satisfied. The output pulse duration is given by $T = \tau_1 \log_e(2)$ where $\tau_1 \approx CR$ with $R \gg R_c$. Experimental values of C is 0.0082 micro-farad with $C_T = 0.1$ micro-farad and $R_T = 100$ K.

A_7 - The Sampling Gate:

The sampler circuit is shown in Fig. 22. When a the control voltage at the point P_1 is -4V and at point P_2 is +20V, the diodes D_1, D_2, D_3, D_4 are cut off and D5 and D6 are

conducting for input signal values between 0 to 16 volts. Current I_1 (through diode D_5) = $(28 - \Delta V)/R$ where ΔV is the drop across the conducting diode. Current I_1' through D_6 is $(44 - \Delta V)/R$.

Similarly when the control voltages at P_1 and P_2 are +20 volts and -4 volts respectively, the diodes D_5 and D_6 are cut off and diodes D_1, D_2, D_3, D_4 are conducting for input signals ranging from 0 to +16 volts provided the resultant current through diode D_1 is maintained in its forward direction (BA). Under this condition the current through D_1 in the forward direction is $\frac{1}{2}(B^+ - B^-)/2R$. The current through D_1 due to signal V_s which flows in the reverse direction is $V_s/2R_L$ where R_L is the load resistance. Since the current to be maintained in the diode D_1 is to be in the forward direction, the inequality $\left\{\frac{1}{2}(B^+ - B^-)/2R\right\} > (V_s/2R_L)$ should be satisfied. To achieve this aim, the circuit parameters and potentials are chosen as shown in Fig. 22.

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